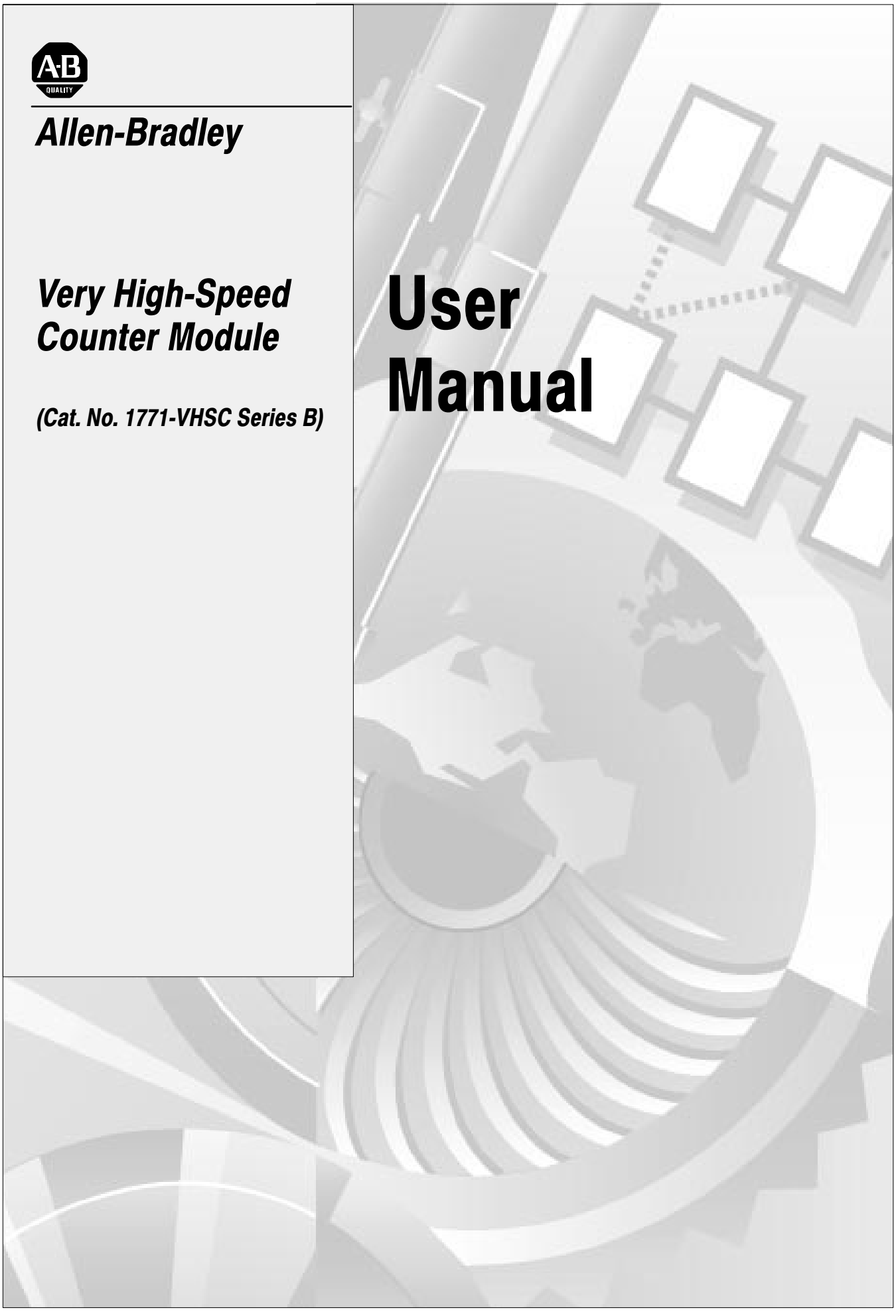


Allen-Bradley

Very High-Speed Counter Module

(Cat. No. 1771-VHSC Series B)

User Manual

Important User Information

Because of the variety of uses for the products described in this publication, those responsible for the application and use of this control equipment must satisfy themselves that all necessary steps have been taken to assure that each application and use meets all performance and safety requirements, including any applicable laws, regulations, codes and standards.

The illustrations, charts, sample programs and layout examples shown in this guide are intended solely for example. Since there are many variables and requirements associated with any particular installation, Allen-Bradley does not assume responsibility or liability (to include intellectual property liability) for actual use based upon the examples shown in this publication.

Allen-Bradley publication SGI–1.1, “Safety Guidelines For The Application, Installation and Maintenance of Solid State Control” (available from your local Allen-Bradley office) describes some important differences between solid-state equipment and electromechanical devices which should be taken into consideration when applying products such as those described in this publication.

Throughout this manual we make notes to alert you to possible injury to people or damage to equipment under specific circumstances.

ATTENTION: Identifies information about practices or circumstances that can lead to personal injury or death, property damage or economic loss.

Attention helps you:

- Identify a hazard.
- Avoid the hazard.
- Recognize the consequences.

Important: Identifies information that is especially important for successful application and understanding of the product.

Important: We recommend you frequently backup your application programs on appropriate storage medium to avoid possible data loss.

Summary of Changes

Summary of Changes

This release of the publication contains new and updated information from the last release.

New Information

This release includes information on the Series B version of the 1771-VHSC module. This includes a new Appendix E on the differences between period/rate and continuous/rate modes of operation. This information was not included in the previous version of this publication.

Updated Information

This release includes updated information in Appendix C, “application Considerations,” and revised Specifications in Appendix A.

Change Bars

To help you find new and updated information in this publication, we have included change bars as shown to the right of this paragraph.

Table of Contents

Using This Manual

Purpose of This Manual

This manual shows you how to use the Very High Speed Counter module with an Allen-Bradley programmable controller. It helps you install, program, and troubleshoot your module.

Audience

You must be able to program and operate an Allen-Bradley programmable controller (PLC) to make efficient use of this module. In particular, you must know how to program your PLC for block transfer-type instructions.

We assume that you know how to do this in this manual. If you do not, refer to the appropriate programming and operations manual for the associated programmable controller before you attempt to use this module.

Vocabulary

In this manual, we refer to:

- the Very High Speed Counter module as the “module,” the “1771-VHSC” or the “VHSC module.”
- the programmable controller as the “controller,” or the “PLC.”

Manual Organization

This manual is divided into six chapters. The following chart shows each chapter with its corresponding title and a brief description of the topics covered in that chapter.

Chapter	Title	Topics Covered
1	Overview of the Very High Speed Counter Module	Explanation of modes, outputs, default configuration and how the module communicates with the processor.
2	Installing the Very High Speed Counter Module	How to install, key, connect wiring, ground and an explanation of the indicators on the module.
3	Module Programming	Block transfer programming and programming examples.
4	Configuring Your Module	Configuration and description of bit/words for block transfer write instructions.
5	Module Status and Input Data	Reading data from the module and bit/word description of the block transfer read.
6	Troubleshooting	Using the indicators for troubleshooting and diagnostic codes.

Chapter	Title	Topics Covered
Appendices		
A	Specifications	Specifications for the VHSC module.
B	Sample Programs	Sample programs for various PLC programs.
C	Application Considerations	Selection of input devices and circuit descriptions.
D	Questions and Answers	Helpful answers to the most asked questions.
E	Period/Rate and Continuous/Rate Examples	Examples of the differences of these 2 modes

Related Products

You can install your input module in any system that uses Allen-Bradley programmable controllers with block transfer capability and the 1771 I/O structure.

Contact your nearest Allen-Bradley office for more information about your programmable controllers.

Product Compatibility

This module can be used with any 1771 I/O chassis. Communication between the module and the processor is bidirectional. The PLC sends module information using block transfer write instructions and the 1771 I/O backplane. The PLC receives module status information through block transfer read instruction and places it in the data table. I/O image table use is an important factor in module placement and addressing selection. The module's data table use is listed in the following table.

Table P.A
Compatibility and Use of Data Table

Catalog Number	Use of Data Table				Compatibility			
	Input Image Bits	Output Image Bits	Read Block Words	Write Block Words	Addressing 1/2 -slot	Addressing 1-slot	Addressing 2-slot	Chassis Series
1771-VHSC Rev. A	8	8	18 max	64 max	Yes	See note	See note	A and B
1771-VHSC Rev. B	8	8	26 max	64 max	Yes	See note	See note	A and B

A = Compatible with 1771-A1, A2, A4 chassis.
B = Compatible with 1771-A1B, A2B, A3B, A4B chassis.
Yes = Compatible without restriction
NOTE: - Restricted to complementary module placement (refer to chapter 2)

Related Publications

For a list of publications with information on Allen-Bradley programmable controller products, consult our publication index SD499.

Overview of the Very High Speed Counter Module

Chapter Objectives

This chapter gives you information on:

- features of the VHSC module
- how the module communicates with programmable controllers.
- how the module operates

Module Description

The VHSC module performs high speed counting for industrial applications. The module is an intelligent block transfer I/O module that interfaces signals with any Allen-Bradley programmable controller that has block transfer capability. Block transfer programming moves module status data from the module's memory to a designated area in the processor data table. It also moves configuration words from the processor data table to the module memory.

The VHSC module is a single-slot module that does not require an external power supply. (**Note:** The outputs **do** require a power supply.) After scanning the inputs and updating the outputs, the input data is converted to a specified data type in a digital format to be transferred to the processor's data table on request. Command and configuration data is sent from the programmable controller data table to the module with a BTW instruction.

Features of the Module

The VHSC module counts pulses from encoders (such as Allen-Bradley Bulletin 845H, K, F, P, E and L), pulse generators or mechanical limit switches, proximity switches, etc. and returns either a count or frequency in binary or BCD format.

The module's features include:

- 4 input channels configurable for encoder mode, counter mode, period/rate mode and continuous/rate mode
- 8 outputs, isolated in groups of 2
- outputs are current-sourcing at 5 to 24V dc (2A maximum per output)
- single-ended or differential inputs
- 2-phase encoder inputs up to a frequency of 250KHz
- single-phase counter inputs up to a frequency of 1MHz
- input voltage range of 5 to 24V dc

- returns in status either count or frequency in binary or BCD format
- input counts as high as 999,999
- up to 500KHz in period/rate or rate measurement frequency modes
- outputs can be tied to any counter
- each output has a user-selectable on-off value
- outputs can be tied back to an input for cascading
- automatic default configuration
- each counter has a user-selectable preset and rollover value
- period/rate w/periodic outputs and period/rate w/dynamic outputs can be used for totalization

The 1771-VHSC module operates in the following modes:

- counter mode
- encoder X1 mode
- encoder X4 mode
- period/rate mode
- rate measurement frequency mode
- continuous/rate mode

The operation of the module in these modes is described below.

Operation in Encoder or Counter Mode

The operation of encoder and counter modes is virtually identical. The only difference between the two modes is in the type of feedback used.

Use the counter mode if you need the module to read incoming pulses from a maximum of four encoders (single-ended or differential), counters, pulse generators, mechanical limit switches, etc. and return them to the programmable controller as a binary or BCD number (0-999,999). In counter mode, the module accepts only one channel feedback.

Use the encoder modes if you need the module to read incoming quadrature pulses and return them to the programmable controller as a binary or BCD number (0-999,999). In these modes, the module accepts two-phase quadrature feedback and counts up or down depending upon the condition of the phase B input for each counter.

The operation of the module in the encoder/counter modes is as follows:

- counter mode - channel B is tied high or low. Channel A input is used for pulse. The count is unidirectional with the direction determined by
  channel B.
- encoder X1 - This is a bidirectional count mode; counting up or down, using quadrature input signals.
- encoder X4 - This is a bidirectional count mode, using quadrature input signals, with 4 times the resolution of X1.

Each of the counters in encoder/counter mode has values associated with it. These are:

- preset value
- rollover value
- gate/reset input
- output

Counter Mode

The counter mode allows the module to read incoming pulses and return them to the programmable controller processor as a binary or BCD number (0-999,999).

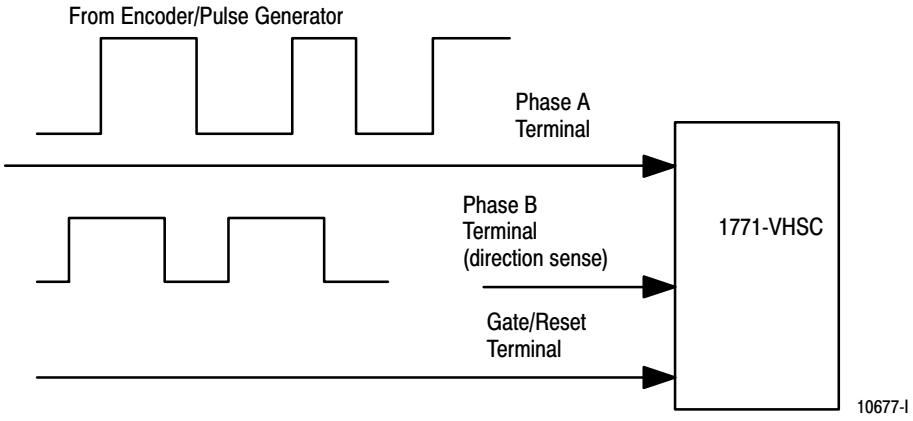
In the counter mode, direction (up counting or down counting) is determined by the phase B input, which can be a random signal. If Phase B is high, the counter will count down. If phase B is low or floating, (that is, not connected), the counter counts up.

If Phase B is:	Counter will count (direction):
High	Down
Low or floating (not connected)	Up

The module reads incoming pulses from a maximum of 4 encoders (single-ended or differential), counters, pulse generators, mechanical limit switches, and so forth and returns a count to the programmable controller processor in a binary or BCD number (0-999,999).

The counter mode accepts only one phase feedback. This relationship is shown in 1.1.

Figure 1.1
Block Diagram of Counter Mode



Encoder Mode

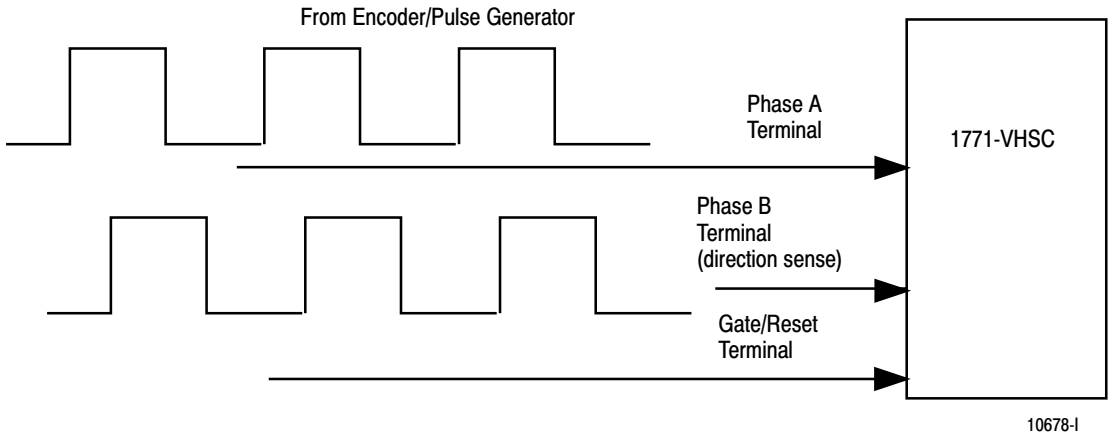
The encoder mode allows the module to read incoming pulses and return them to the programmable controller processor as a binary or BCD number (0-999,999).

In this mode, the module will accept two phase quadrature feedback. The module senses the relationship between the 2 phases and counts up or down accordingly.

Encoder X1 mode uses channel A for the pulse input. With B low (floating), the count direction is up; when B is high, the count direction is down.

Encoder X4 mode is identical to X1, except it uses quadrature signals on channel A and channel B, and counts on the leading and trailing edges of
A and B.

Figure 1.2
Block Diagram of Encoder Mode

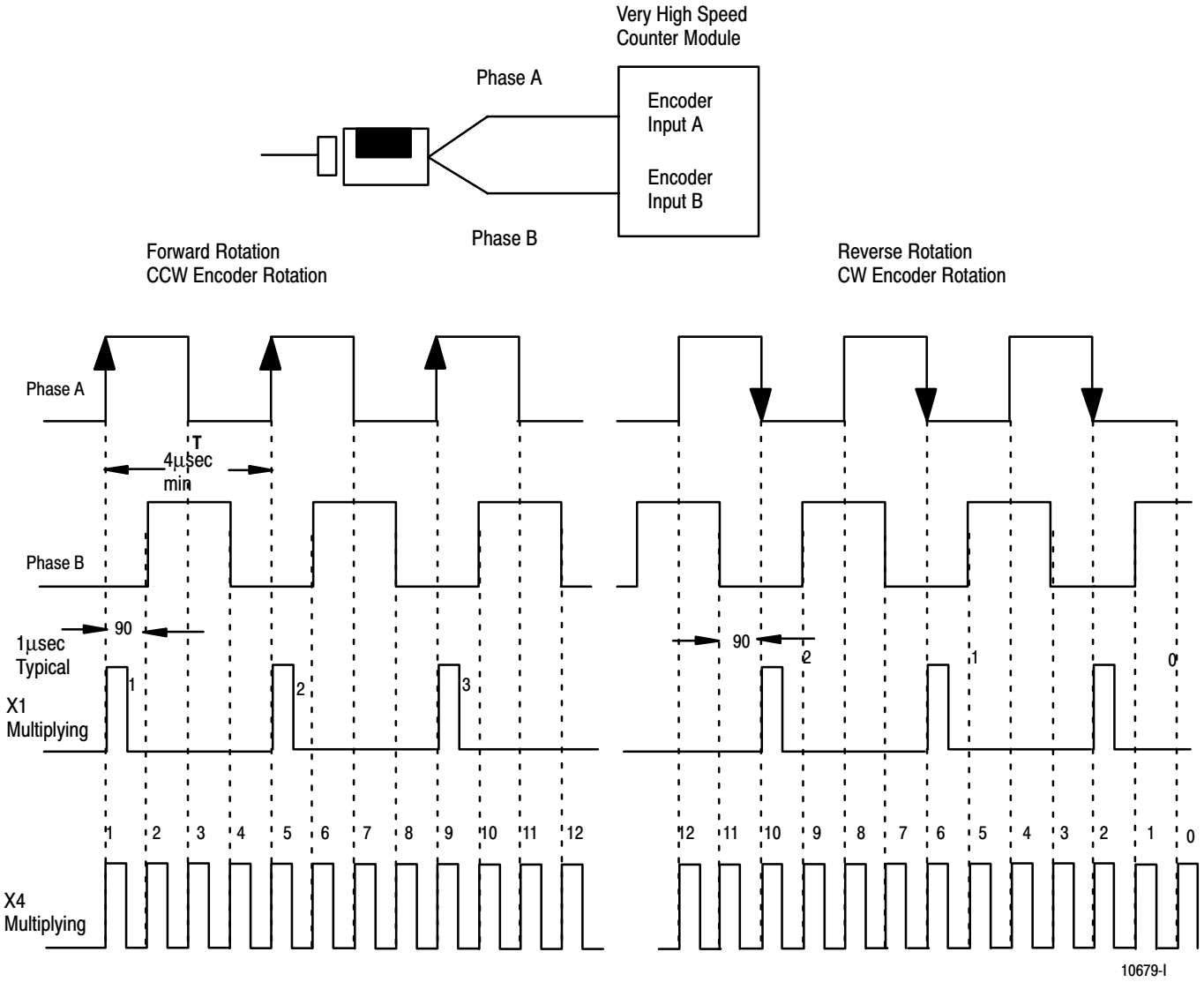


Direction of Count

The module can count either up or down, depending upon the condition of the B input for each counter. In encoder applications, the counter will increment on the leading edge of Phase A, while phase B determines the direction of the count.

You also have the option of X1 and X4 multiplying of the input pulses. 1.3 shows the relationships between phases A and B for forward and reverse directions in encoder applications.

Figure 1.3
Phase Relationship for Forward or Reverse Directions



The following paragraphs apply to both encoders and counters.

Preset Value

Each of the 4 counters has one preset value associated with it. In the encoder or counter modes, the preset value represents a reference point (or count) from which the module begins counting. The module can count either up or down from the preset value. Preset values are loaded into the count registers through the preset count bits. (Refer to word 1, bits 8-11 of the block transfer write initialization block in chapter 5.) Preset values can range from 0 to 999,999 binary or BCD.

Rollover Value

Each of the 4 counters has one rollover value associated with it. When the rollover value is reached by the encoder/counter, it resets to 0 and begins counting again. The rollover values range from 0 to 999,999 binary or BCD (0 represents 1,000,000). The rollover value is circular (for example: if you program 360, the count will be from 358, 359, 0, 1 etc. in a positive direction and from 1, 0, 359, 358 etc. in a negative direction).

Software Reset

The counters can also be reset by the Reset Count bits found in Word 1, bits 0-3 of the block transfer write. When one of these bits is set to 1, the associated counter is reset to zero and begins counting. The module can also be reset with the gate/reset as explained below. Refer to chapter 4 for further details.

Gate/Reset Input

There is one gate/reset input for each of the 4 counters. The gate/reset input, when active, will function in one of the 4 store count modes outlined below.

Scaling Input Count at the Gate/Reset Terminal
You can scale the incoming count at the gate/reset terminal. Scaling allows the incoming pulses at gate/reset to be divided by a number in the range of 1, 2, 4, 8, 16, 32, 64 and 128. Refer to words 21 to 24 in the BTW file (chapter 4).

Store Count
The store count feature allows the module to store the current count value of any (or all) of the four counters. The store count feature is triggered by the state of the gate/reset terminal on the module. The stored count of each counter is placed in a separate word in the Block Transfer Read file (words 11-18 respectively). The stored count value will remain in the block transfer read file until a new trigger pulse is received at the Gate/Reset terminal. When a new trigger pulse is received, the old count value will be overwritten by the new value.

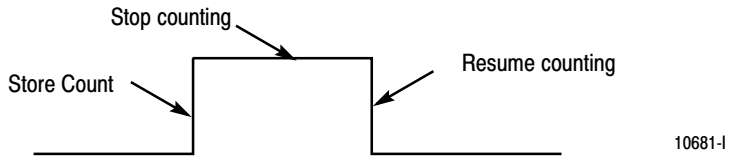
The store count feature is selected by words 3 and 4 of the block transfer write initialization file. Refer to chapter 4 for further details.

In **mode 1, store/continue** (1.4), the leading edge of a pulse input on the gate/reset terminal will cause the current value in the counter to be read and stored. The counter will continue counting. The stored count will be available in the block transfer read file. The stored count information will remain in the block transfer read file until it is overwritten by new data.

Figure 1.4
Store/Continue

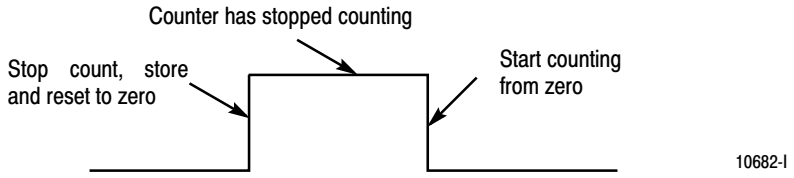
In **mode 2, store/wait/resume** (1.5), the gate/reset terminal provides the capability to inhibit counting when the gate/reset input is high. Counting resumes when the input goes low. Mode 2 does not reset the counter, although it does store the count value.

Figure 1.5
Store/Wait/Resume



In mode 3, store-reset/wait/start (1.6), the rising edge of the pulse on the gate/reset terminal causes the counter to stop counting, store the current count value in the block transfer read file and reset the count to zero. The counter does not count while the input pulse on the gate/reset terminal remains high. Counting resumes from zero on the falling edge of the pulse at the gate/reset terminal.

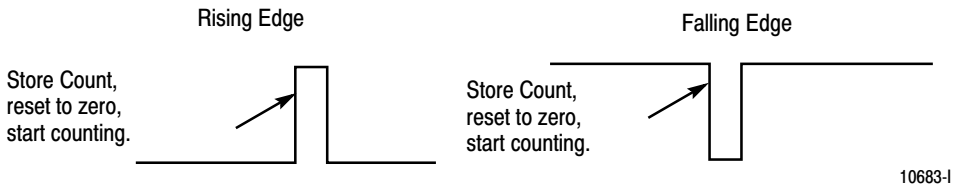
Figure 1.6
Store-Reset/Wait/Start



In **mode 4, store-reset/start** (1.7), on the rising edge of a pulse input at the gate/reset terminal will cause the counter to store the accumulated count value and will reset the counter to zero. The counter continues counting, and the stored count is available in the block transfer read file.

Figure 1.7

Store-Reset/Start



Figures 1.4 through 1.7 show the store count feature operating on the rising edge of the gate/reset pulse. The user has the option of selecting these same features using the falling edge of the gate/reset pulse. This selection is made through the gate invert bit as explained in chapter 4.

The gate invert bit is active in the store count, continuous/rate and period/rate modes.

The stored count values are saved in words 11 through 18 of the block transfer read file (chapter 4).

Operation in Period/Rate Mode

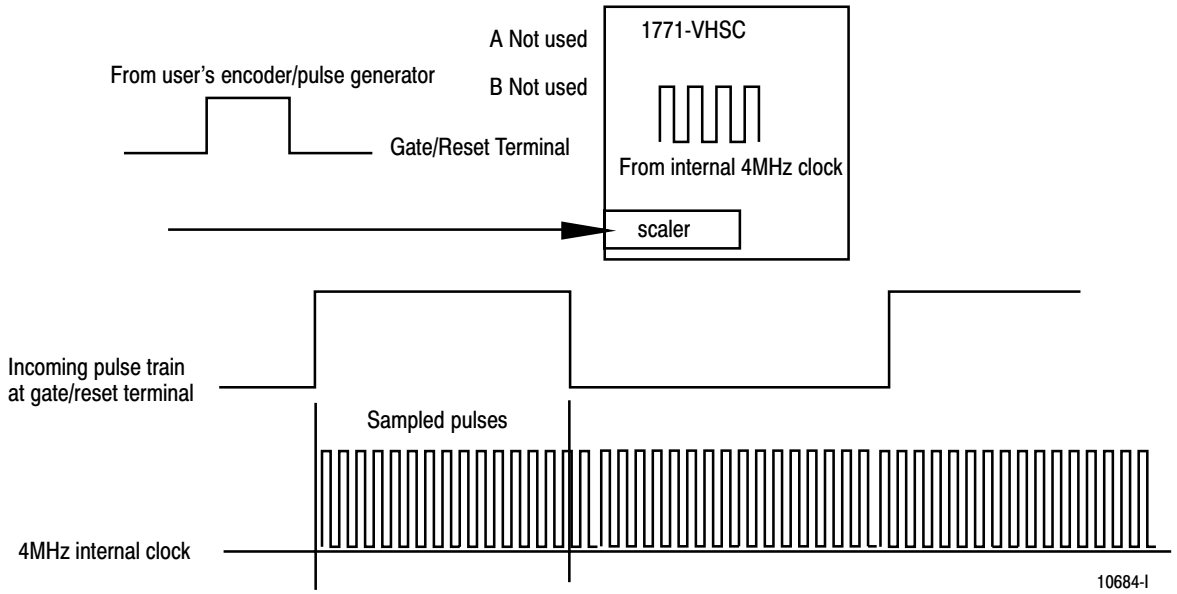
Use the period/rate mode to determine the frequency of input pulses by counting the number of internal 4MHz clock pulses over a user-specified number of input signal pulses. At the end of the specified number of pulses, the module returns the frequency and the number of internal 4MHz pulses.

A channel configured for period/rate mode acts as a period rate counter. An internal 4 MHz clock is used as a frequency reference. This clock is gated by the incoming pulse train at the gate/reset input. The results of this gating action are the number of pulses or a frequency. The number of sampled gated 4MHz pulses are returned in BTR words 3 thru 10, and the frequency in words 11 thru 18. Select the period/rate mode by setting the appropriate bits in words 3 and 4 of the BTW initialization file (chapter 4). The store count features are inactive in period/rate mode.

1771-VHSC revision B and later modules count the total number of pulses occurring at the gate/reset pin. This function is frequency-limited. This total count is returned when you request words 19 through 26 in your BTR. You can reset this count by resetting the reset bit (bits 0-4 in BTW word 1). Rollover and preset are inactive. Refer to appendix E for additional information.

1.8 shows a diagram of the module used in the period/rate mode.

Figure 1.8
Period/Rate Mode



In 1.8, the incoming pulse train from the gate/reset terminal is used to sample pulses from the 4 MHz internal clock. As the frequency of the incoming pulse train at the gate/reset terminal increases, the number of sampled pulses from the 4 Mhz clock decreases. This relationship is shown in Table 1.A. Since accuracy is related to the number of pulses received over the sample period, the accuracy will decrease with increasing input frequencies at the Gate/Reset terminal. To some extent, the decrease in accuracy can be lessened by scaling the input frequency through the use of a scaler. A scaler value of 1 will only return an accurate input frequency if incoming pulses have a 50% duty cycle. If frequency exceeds 500KHz, the number 999,999 is returned.

Table 1.A
Relationship Between Sampled Pulses and Input Frequency

Input Frequency at Gate/Reset Terminal in Hz (words 11-18 in BTR)	Sampled Pulses for 1/2 Cycle of Gate/Reset Pulse (words 3-10 in BTR)
2	1 meg
5	400K
10	200K
20	100K
50	40K
100	20K
200	10K
500	4K
1KHz	2K
2KHz	1K
5KHz	400
10KHz	200
20KHz	100
50KHz	40
100KHz	20
200KHz	10

Operation of scaler

In period/rate mode, the scaler lets the incoming pulse train at the gate/reset pin be divided by a user defined number. Acceptable values for the scaler are 1, 2, 4, 8, 16, 32, 64 and 128. There is one scaler value for each counter. The default value for each scaler is 1.
Note: A 0 is equivalent to 1.

ATTENTION: Sample period times scaler must be less than 0.25 seconds or the counter will overflow without providing an overflow indication.

Connection to Counter Inputs

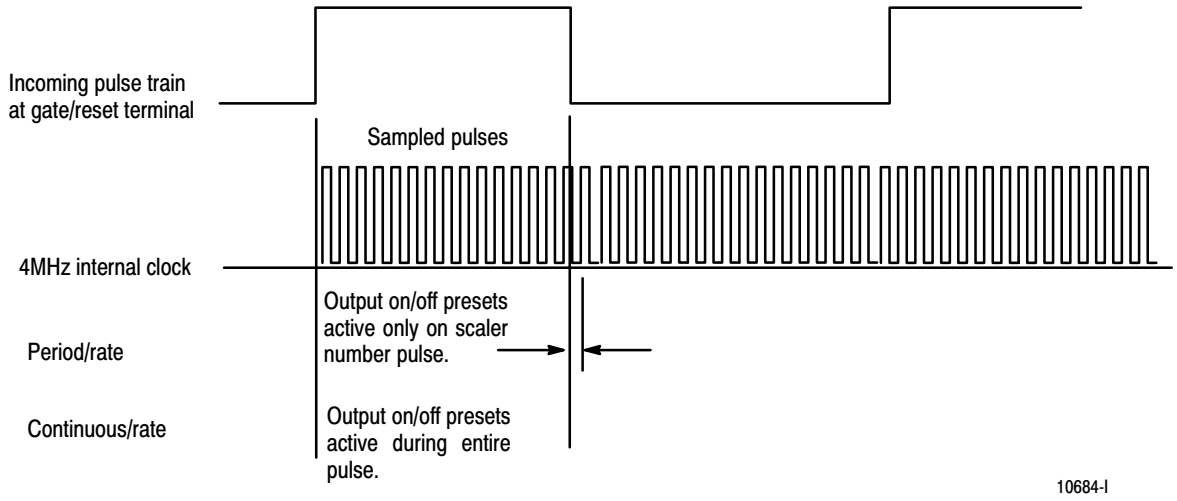
The only input to the module in the period/rate mode is made to the gate/reset terminal. The counter inputs (channel A and B) are not used in the period/rate mode.

Continuous/Rate Mode

The continuous/rate mode is similar to the period/rate mode previously described except the outputs in this mode are dynamic outputs. Use this mode to determine the frequency of input pulses by counting the number of internal 4MHz clock pulses over a user-specified number of input signal pulses. Each output is turned on as soon as the turn-on count is reached, and turned off as soon as the turn-off count is reached. As the internal 4MHz clock is counted, the outputs dynamically track the 4MHz count. This allows you to turn an output on a certain number of 4MHz counts after the gate/reset pin goes active, and turn it off a certain number of 4MHz counts later.

1771-VHSC revision B and later modules count the total number of pulses occurring at the gate/reset pin. This function is frequency-limited. This total count is returned when you request words 19 through 26 in your BTR. You can reset this count by resetting the reset bit (bits 0-4 in BTW word 1). Rollover and preset are inactive. Refer to appendix E for additional information.

Figure 1.9
Period/Rate and Continuous/Rate Output Operation with Scaler of 1

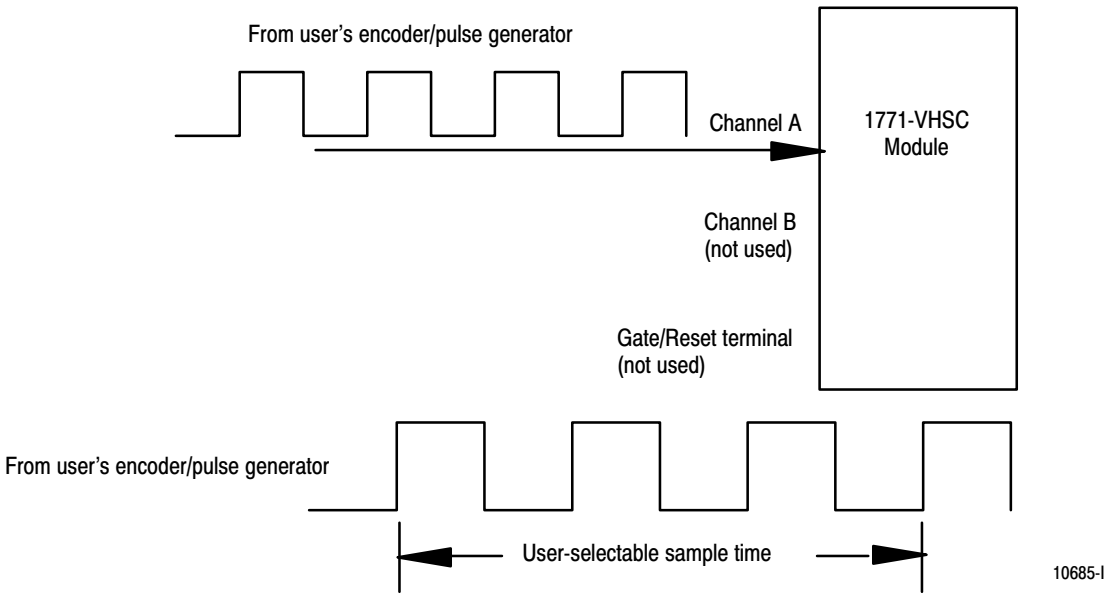


Operation in Rate Measurement Mode

Use the rate measurement mode to count incoming pulses for a user-specified time interval. At the end of the interval, the module returns a value representing the sampled number of pulses and a value indicating the incoming frequency. When the count and frequency are updated, any associated outputs are checked against their associated presets.

The value representing the sampled number of pulses is returned in BTR words 3 thru 10, and the value indicating the incoming frequency is returned in words 11-18. The total count equals the number of pulses received during the sample period. The operation of rate measurement mode is shown below in 1.10.

Figure 1.10
Operation of the Rate Measurement Mode



Example:
In 1.10, three counts have been accumulated during the user-selected time period. If you had selected 50 milliseconds as the sample period, the frequency returned to the programmable controller processor in words 11-12 would be:

Frequency = Counts/Sample period = 3 counts/50 milliseconds = 60 Hz

You would read 60 Hz as the frequency in the Block Transfer Read file (words 11 and 12). Words 3 and 4 would contain the value 3. Since the default configuration for the VHSC module is the Counter mode, the user must select the rate measurement mode through the block transfer write initialization file. This is done by setting the appropriate bits in words 3 and 4 of the block transfer write initialization file (chapter 4). If frequency exceeds 500KHz, the number 999,999 is returned.

Sample Period
You can set the sample period used in the frequency calculation in the rate measurement mode. Allowable values are 10 milliseconds to 2 seconds in 10 millisecond increments. The default value is 1 second. (**Note:** A 0 in the BTW initialization word is equivalent to the default value of 1 second.)

The sample period is set in words 21 through 24 of the BTW initialization file (chapter 4).

Connection to Counter Inputs
The only user connections used in the rate measurement mode are to phase A of the module. The gate/reset and channel B terminals are not used in this mode.

Outputs

The VHSC module has 8 outputs, isolated in groups of 2. Each of the outputs is capable of sourcing current and will operate between 5 and 24 volts dc. You must connect an external power supply to each of the outputs. The outputs can source 2 amps dc. The outputs are hardware-driven and will turn on in less than 10µsec when the appropriate count value has been reached.

Enabling and Forcing Outputs

Outputs may be forced on or off independent of count or frequency value. To force the outputs, they must first be enabled. Enabling the outputs is done through a data table word 2, bits 0-7 in the BTW initialization file (chapter 4). Once the outputs have been enabled, they may be forced on by setting bits 8-15 in word 2 of the BTW initialization file. The outputs can be forced off by setting the enable bit to 0.

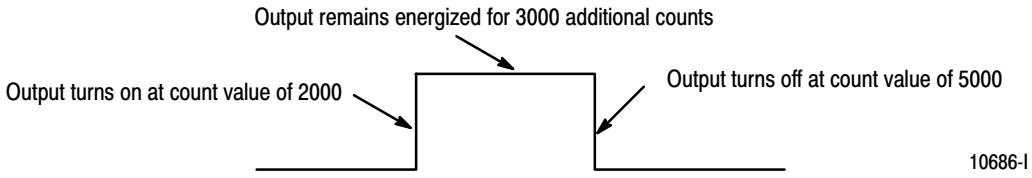
Assigning Outputs to Counters

By setting bits in the block transfer write initialization file, you can assign the outputs on the module to any of the various counters. You can assign as many as 8 outputs to a given counter. However, an output may be assigned only once to a counter--it is not possible to use the same output with 2 different counters. Refer to words 25, 30, 35, 40, 45, 50, 55, 60 of the BTW initialization file in chapter 4.

Operation of Outputs

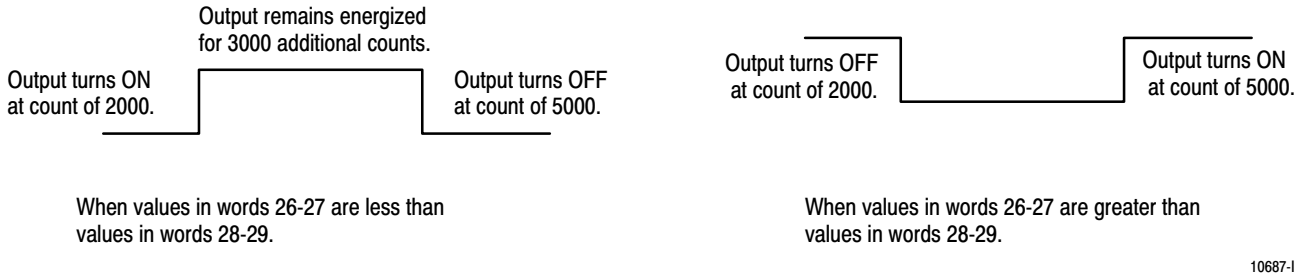
When the outputs for the VHSC module are enabled and assigned to a counter they operate in an ON-OFF fashion. For example, assume that the module were programmed to turn ON an output when a count value of 2000 was reached. Further, assume that the user desired to have the output remain energized for a period of 3000 counts and then turn OFF. The end result would be that the outputs would turn ON at count of 2000, would remain energized for 3000 additional counts, and would turn OFF at 5000 counts. The ON and OFF values are circular around zero. In the rate measurement mode, the On and Off values associated with each output represent a frequency value instead of a count value. The maximum frequency value which may be entered in an On or Off value is 500,000Hz. Refer to 1.11.

Figure 1.11
On-Off Operation of Output



Refer to 1.12. Using output 0 as an example, when the value in words 26 and 27 is less than the value in words 28 and 29, the output turns on at 2000 and off at 5000. If the value in words 26 and 27 is greater than the value in words 28 and 29, the output turns off at 2000 and on at 5000.

Figure 1.12
Effect of Values in Words 26 through 29



Refer to words 26-29, 31-34, 36-39, 41-44, 46-49, 51-54, 56-59, 61-64 of the block transfer write initialization file in chapter 5.

Isolation of Outputs

The module provides 1500V ac forced rms isolation between each of the counters and the backplane of the I/O rack.

Tying Outputs to Counters

You can jumper any of the outputs to any of the counter inputs on the module field wiring arm. In this way, it is possible to use the outputs to reset a counter or to cascade counters. If using the outputs this way, make certain that the input voltage jumpers are set to interface with the appropriate output voltage.

Handshaking

A pair of handshaking bits are provided for each counter. These bits are called New Data (ND) bits in the BTR instruction, and New Data Acknowledge (NDA) bits in the BTW instruction. They indicate when a stored data value has been most recently updated. These bits are provided for count/accumulate applications, but can be used whenever the stored data is updated at a rate slower than the block transfer time.

The New Data bit (BTR status word 1, bits 4-7 for counters 0-3 respectively) can be used by the ladder program to indicate that a store register (BTR words 11-18) has been updated by one of the following events:

- An active gate transition in any of the **store count modes**
- The end of the gate sample period in either the **period/rate or continuous/rate modes**
- The end of the programmed sample period in **rate measurement mode**

The ND bit is reset in the ladder program by a 0 to 1 transition of the corresponding NDA bit, and then performing a BTW. A BTW length of 1 word can be use for this handshaking procedure.

Note: A BTW length of 1 has no effect on the preset or reset bits in BTW word 1, and does not qualify as a configuration BTW. (For example, if the BTW valid bit is set, it will remain set after the BTW with a length of 1 is sent.)

Default Configuration

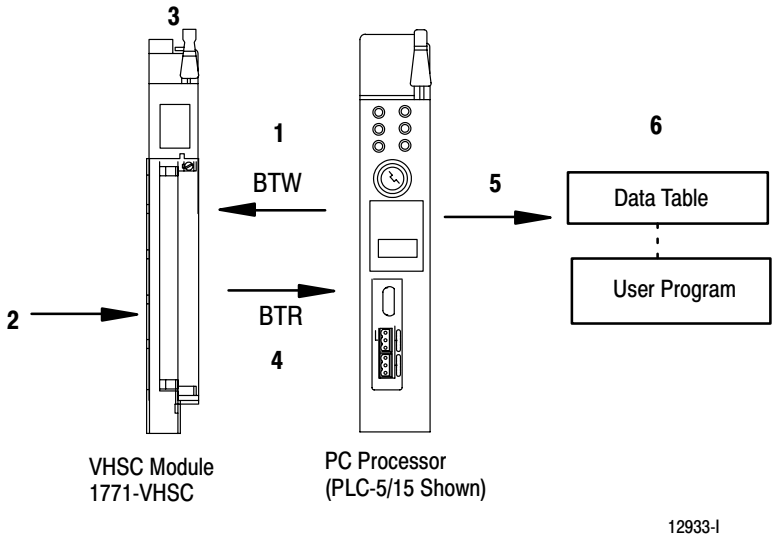
A default configuration is built into the module. The default configuration is automatically selected on power-up if the user has not configured the module through a Block Transfer Write Initialization file. The module can be placed in the default configuration by writing a block transfer write initialization file with all zeroes to the module.

The default mode for the VHSC module is the counter mode for all 4 of the counters. In the default configuration, the module will continuously return counts (0-999,999 binary) to the programmable controller processor. The presets and rollovers associated with each of the 4 counters will not be active, nor will any of the outputs be active.

How the Module Communicates with a Programmable Controller

The processor transfers data to and from the module using block transfer write (BTW) and block transfer read (BTR) instructions in your ladder diagram program. These instructions let the processor obtain input values and status from the module, and let you establish the module's mode of operation (1.13).

Figure 1.13
How the Module Communicates with a Programmable Controller



1. The processor transfers your configuration data and commands to the module using a BTW instruction.
2. External devices generate input signals that are transmitted to the module.
3. The module converts these signals into binary or BCD format, and stores these values and controls their output until the processor requests their transfer.
4. When instructed by your ladder program, the processor performs a BTR of the values and stores them in a data table.
5. The processor and module determine that the transfer was made without error, and that input values are within a specified range.

6. Your ladder program can use/or move the data (if valid) before it is written over by the transfer of new data in a subsequent transfer.

Chapter Summary

In this chapter you learned how your module operates, and how your module communicates with the programmable controller.

Installing the Very High-Speed Counter Module

Chapter Objectives

This chapter gives you information on:

- calculating the chassis power requirement
- keying a chassis slot for your module
- setting the voltage and filter jumpers
- wiring the input module's field wiring arm
- installing the input module

Before You Install Your Module

Before installing your module in the I/O chassis you must:

Action required:	Refer to:
Calculate the power requirements of all modules in each chassis.	Power Requirements
Determine where to place the module in the I/O chassis.	Module Location in the I/O Chassis
Key the backplane connector in the I/O chassis.	Module Keying
Make connections to the wiring arm.	Connecting Wiring and Grounding

European Union Directive Compliance

If this product is installed within the European Union or EEA regions and has the CE mark, the following regulations apply.

EMC Directive

This apparatus is tested to meet Council Directive 89/336/EEC Electromagnetic Compatibility (EMC) using a technical construction file and the following standards, in whole or in part:

- EN 50081-2 EMC – Generic Emission Standard, Part 2 – Industrial Environment
- EN 50082-2 EMC – Generic Immunity Standard, Part 2 – Industrial Environment

The product described in this manual is intended for use in an industrial environment.

Low Voltage Directive

This apparatus is also designed to meet Council Directive 73/23/EEC Low Voltage, by applying the safety requirements of EN 61131–2 Programmable Controllers, Part 2 – Equipment Requirements and Tests.

For specific information that the above norm requires, see the appropriate sections in this manual, as well as the following Allen-Bradley publications:

- Industrial Automation Wiring and Grounding Guidelines, publication 1770-4.1
- Guidelines for Handling Lithium Batteries, publication AG-5.4
- Automation Systems Catalog, publication B111

Electrostatic Damage

Electrostatic discharge can damage semiconductor devices inside this module if you touch backplane connector pins. Guard against electrostatic damage by observing the following warning:

ATTENTION: Electrostatic discharge can degrade performance or cause permanent damage. Handle the module as stated below.

- Wear an approved wrist strap grounding device when handling the module.
- Touch a grounded object to rid yourself of electrostatic charge before handling the module.
- Handle the module from the front, away from the backplane connector. Do not touch backplane connector pins.
- Keep the module in its static-shield bag when not in use, or during shipment.

Power Requirements

Your module receives its power through the 1771 I/O chassis backplane from the chassis power supply. The maximum current drawn by the module from this supply is 650mA (3.25 Watts).

Add this value to the requirements of all other modules in the I/O chassis to prevent overloading the chassis backplane and/or backplane power supply.

Module Location in the I/O Chassis

Place your module in any slot of the I/O chassis except for the extreme left slot. This slot is reserved for processors or adapter modules.

When using:	You can:
2-slot addressing	place your module in any module group with any 8-bit or block transfer module.
1-slot addressing	place your module in any module group with any 8-bit, 16-bit or block transfer module.
1/2-slot addressing,	no restrictions on module location.

After determining the module's location in the I/O chassis, connect the wiring arm to the pivot bar at the module's location.

Module Keying

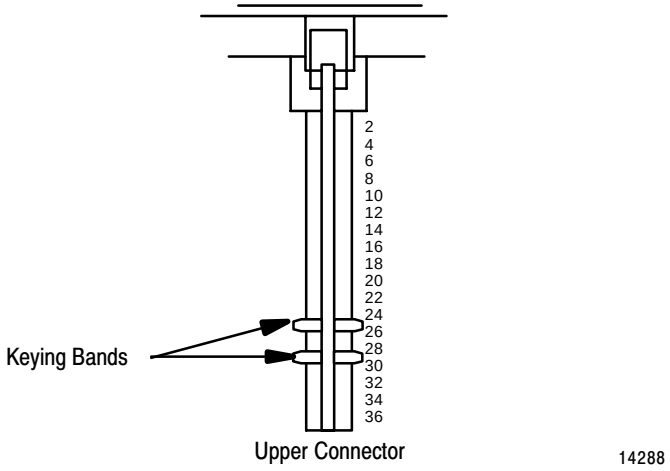
Use the plastic keying bands, shipped with each I/O chassis, for keying the I/O slot to accept only this type of module.

The module is slotted in two places on the rear edge of the circuit board. The position of the keying bands on the backplane connector must correspond to these slots to allow insertion of the module. You can key any connector in an I/O chassis to receive these modules except for the leftmost connector reserved for adapter or processor modules. Place keying bands between the following numbers labeled on the backplane connector (Figure 2.1):

- Between 24 and 26
- Between 28 and 30

You can change the position of these bands if subsequent system design and rewiring makes insertion of a different type of module necessary. Use needlenose pliers to insert or remove keying bands.

Figure 2.1
Keying Positions



Setting the Configuration Jumpers

The VHSC module has user-selectable jumpers for each input channel. These jumpers consist of one each:

- filter or high speed operation jumper
- +5V or +12-24V operation jumper

Each counter has a total of 6 jumpers associated with it:

- Channel A filter/high speed jumper
- Channel A voltage jumper
- Channel B filter/high speed jumper
- Channel B voltage jumper
- Gate/reset filter/high speed jumper
- Gate/reset voltage jumper

These jumpers can be set independent of each other. You can select the filter action and voltage for each channel and for the gate/reset input independently.

The high speed operation is the preferred mode of operation for the 1771-VHSC module. Use this mode when the inputs are driven by devices such as encoders or line drivers.

Use the filter mode on the inputs when a mechanical switch is providing the input. The filter provides de-bouncing for the mechanical switch. The frequency of counting must be less than 100Hz when the filter mode is selected.

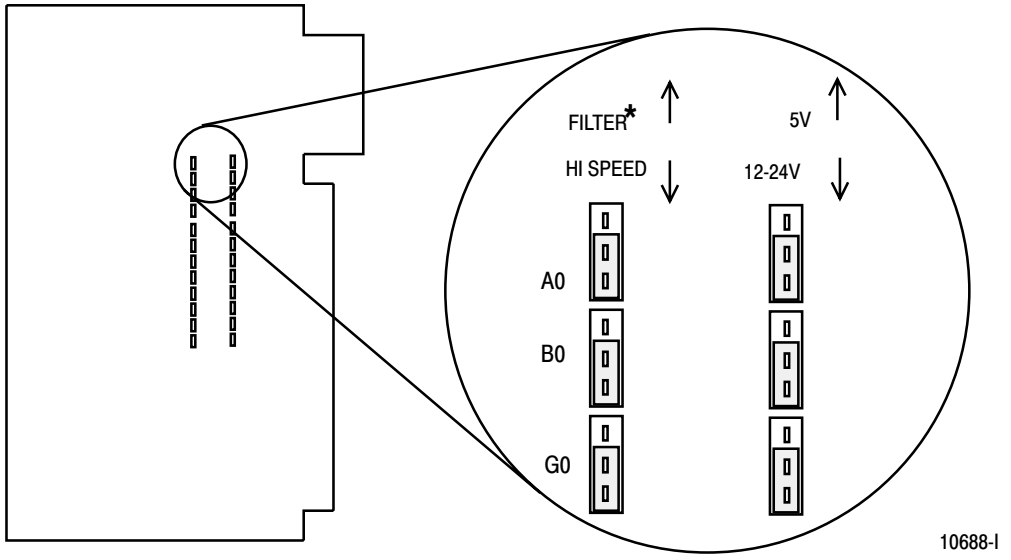
Use these jumpers to match the operation of the module with the input supplied. Settings are shown in Figure 2.2.

To set the jumpers, proceed as follows:

1. Remove the four screws securing the side cover to the module and remove the covers.
2. Using your fingers, reposition the jumpers associated with each input channel according to your requirements. Refer to Figure 2.2.

Figure 2.2
Setting the Configuration Jumpers

Filter Jumper Position	Voltage Jumper Position	Description of Operation
Down	Down	12-24V High Speed (factory default setting)
Down	Up	5V High Speed
Up	Down	12-24V with low speed filter
Up	Up	5V with low speed filter



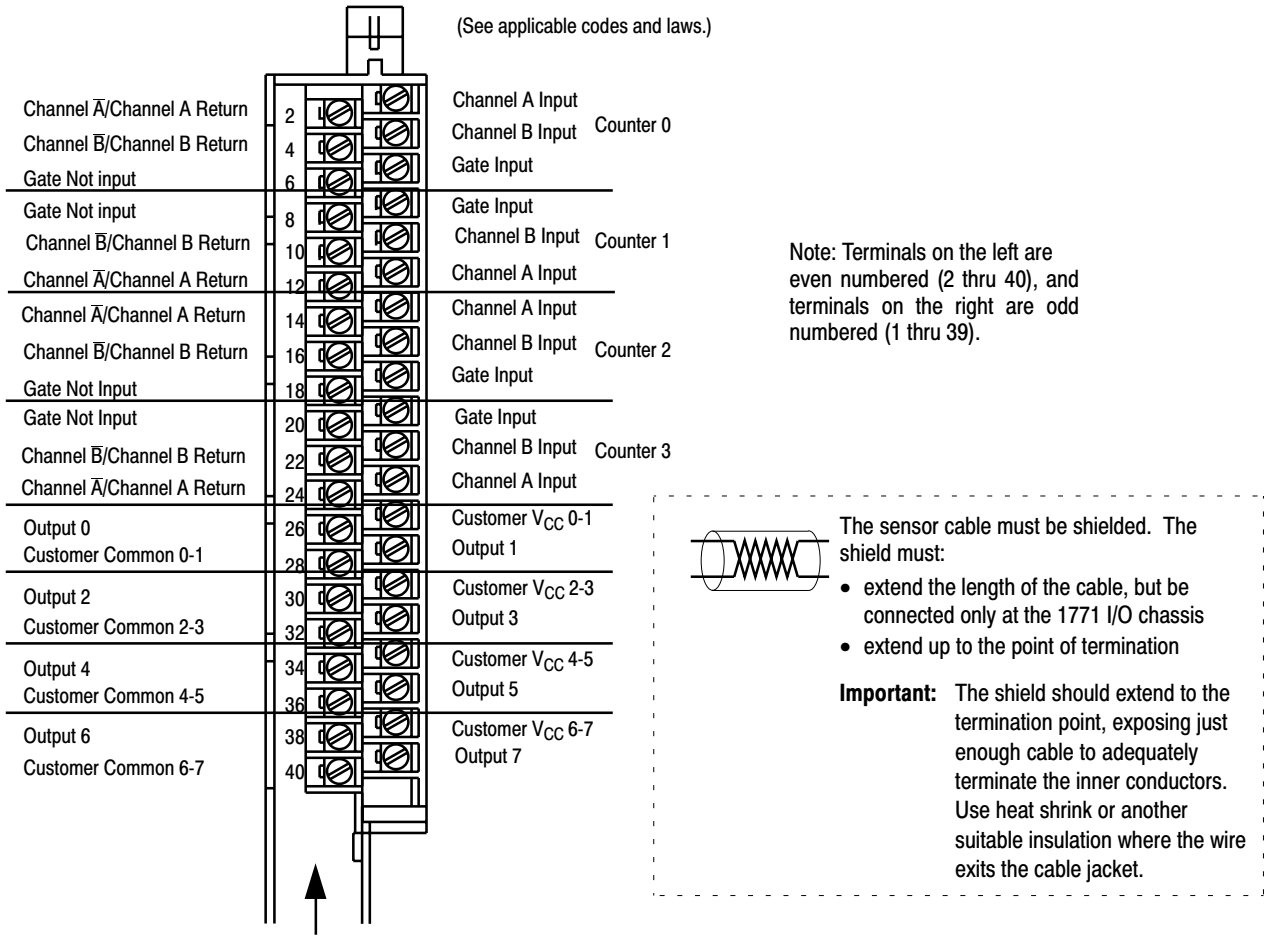
*In the filter position, the module will not see frequencies above 100Hz.

3. Reposition the cover and secure with the 4 screws removed in step 1.

Connecting Wiring

Connect your I/O devices to the 40-terminal field wiring arm (cat. no. 1771-WN) shipped with the module (Figure 2.3). Attach the field wiring arm to the pivot bar at the bottom of the I/O chassis. The field wiring arm pivots upward and connects with the module so you can install or remove the module without disconnecting the wires.

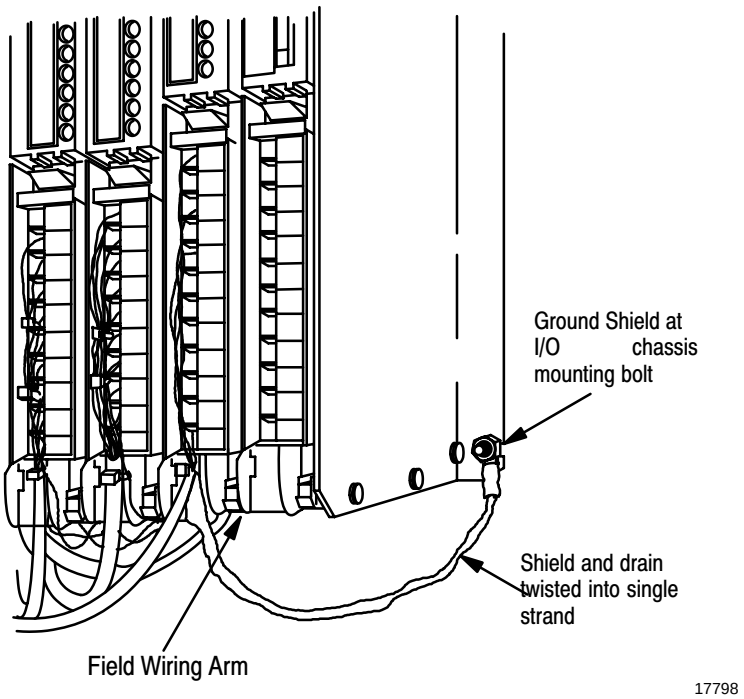
Figure 2.3
Connection Diagram for Very High Speed Counter Module (1771-VHSC)



Grounding the VHSC Module Wiring

When using shielded cable, ground the foil shield and drain wire only at one end of the cable. We recommend that you wrap the foil shield and drain wire together and connect them to a chassis mounting bolt (Figure 2.4). At the opposite end of the cable, tape exposed shield and drain wire with electrical tape to insulate it from electrical contact.

Figure 2.4
Cable Grounding



Refer to Wiring and Grounding Guidelines, publication 1770-4.1 for additional information.

Installing the Module

When installing your module in an I/O chassis:

1. First, turn off power to the I/O chassis:

ATTENTION: Remove power from the 1771 I/O chassis backplane and wiring arm before removing or installing an I/O module.

Failure to remove power from the backplane could cause injury or equipment damage due to possible unexpected operation.

Failure to remove power from the backplane or wiring arm could cause module damage, degradation of performance, or injury.

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2. Place the module in the plastic tracks on the top and bottom of the slot that guides the module into position.
3. Do not force the module into its backplane connector. Apply firm even pressure on the module to seat it properly.

4. Snap the chassis latch over the top of the module to secure it.
5. Connect the wiring arm to the module.

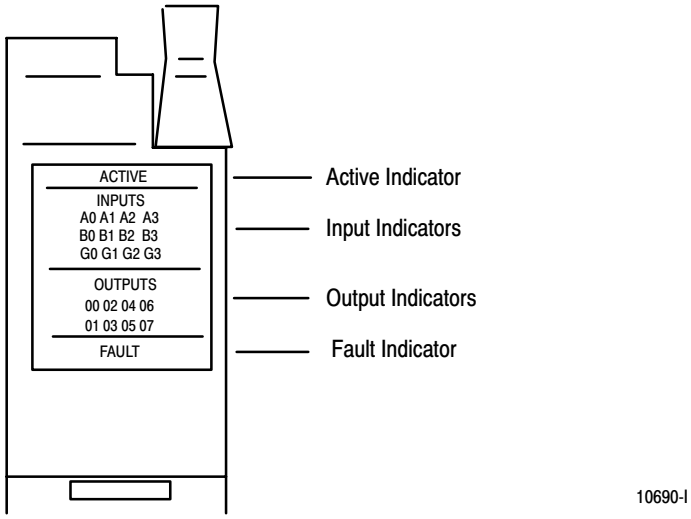
Interpreting the Indicator Lights

The front panel of the input module contains 12 input indicators, 8 output indicators, an active indicator and a fault indicator (Figure 2.5). At power-up, the active and fault indicators are on. An initial module self-check occurs. If there is no fault, the red indicator turns off. If a fault is found initially or occurs later, the fault indicator lights and the active indicator is forced off.

When an input LED (A, B) is on, it indicates that the input is high. When the output LED is on, it indicates that the module has commanded the output to be on. When a gate/reset indicator (G) is on, its input is high. Since that signal can be inverted, it does not indicate whether the signal on that terminal is necessarily logically true.

Possible module fault causes and corrective action are discussed in the chapter titled "Troubleshooting."

Figure 2.5
Diagnostic Indicators



Chapter Summary

In this chapter you learned how to install your input module in an existing programmable controller system and how to wire to the field wiring arm.

Module Programming

Chapter Objectives

In this chapter we describe:

- block transfer programming
- sample programs in the PLC-2, PLC-3 and PLC-5 processors

Block Transfer Programming

Your module communicates with the processor through bidirectional block transfers. This is the sequential operation of both read and write block transfer instructions.

The following example programs accomplish this handshaking routine. These are minimum programs; all rungs and conditioning must be included in your application program. You can disable BTRs, or add interlocks to prevent writes if desired. Do not eliminate any storage bits or interlocks included in the sample programs. If interlocks are removed, the program may not work properly.

Optionally, the block transfer write (BTW) instruction is initiated when the module is first powered up, and subsequently only when the programmer wants to write a new configuration to the module. At all other times the module is basically in a repetitive block transfer read (BTR) mode.

Your module will work with a default configuration of all zeroes entered in the configuration block. See the configuration default section to understand what this configuration looks like. Also, refer to Appendix B for example configuration blocks and instruction addresses to get started.

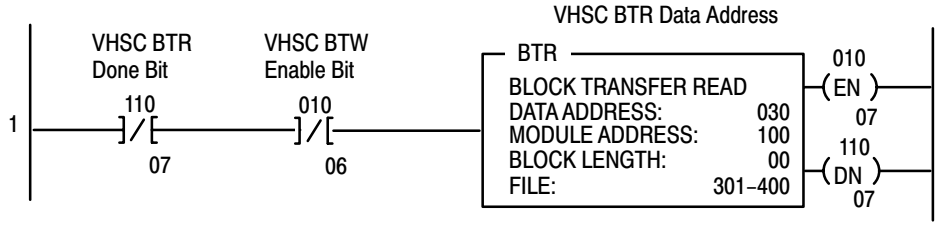
The following example programs illustrate the minimum programming required for communication to take place.

PLC-2 Program Example

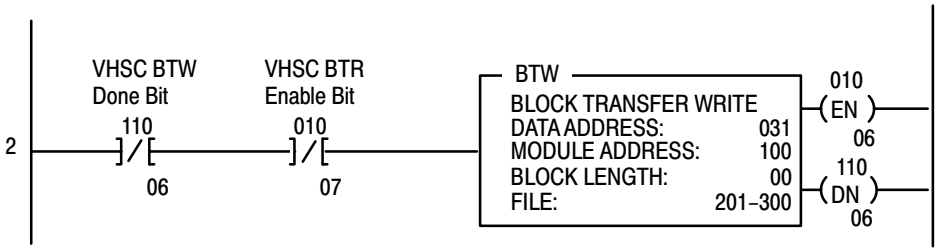
Figure 3.1 below shows a sample PLC-2 program.

Figure 3.1
PLC-2 Family Sample Program Structure

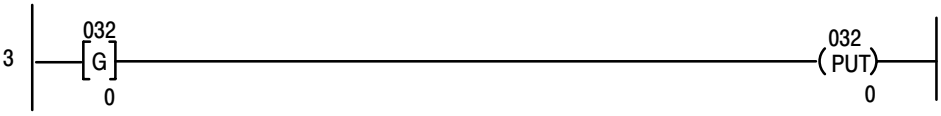
The VHSC module is located in rack 1, module group 0, slot 0. The data address 030 is among the first available timer/counters used for block transfer. The default block length of 0 results in a 18 word block transfer read. The module status data is returned to the processor starting at address 301. If a block length other than 0 is specified for the BTR or BTW the BTR and BTW cannot be enabled during the scan.



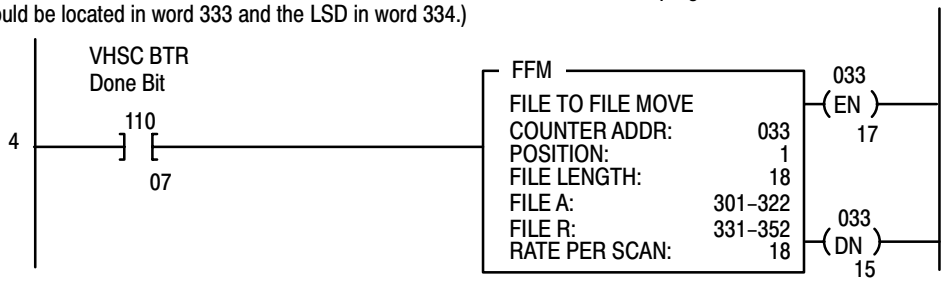
The VHSC module is located in rack 1, module group 0, slot 0. The data address 031 is among the first available timer/counters used for block transfer. The default block length of 0 results in a 64 word block transfer write. The module configuration data is stored starting at address 201. The preconditions could also include the configuration bit (word 1, bit 0) to limit the block transfer write.



This rung is used to place a zero between the first available timer counters used for all block transfers and those used throughout the rest of the program.



This rung uses a BTR done bit to trigger a move of the count data stored at 301 to a buffered location at 331. The program should access all data from the buffered file (count 0 MSD would be located in word 333 and the LSD in word 334.)



PLC-3 Program Example

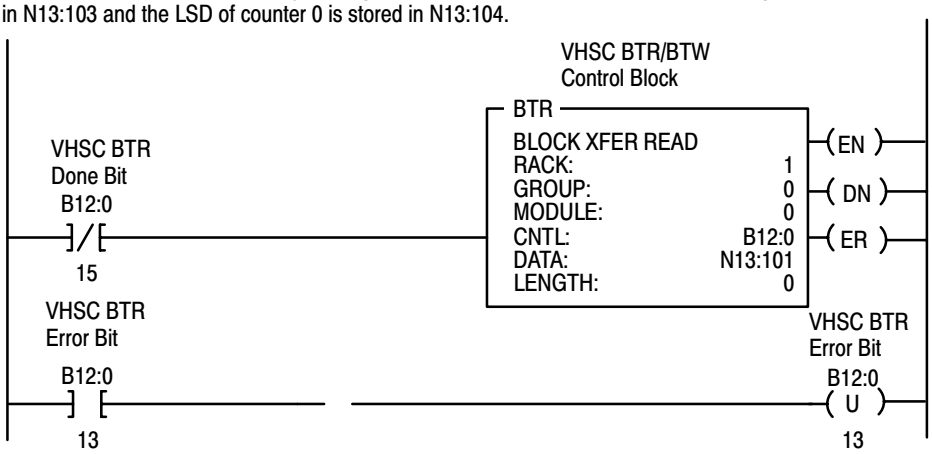
Block transfer instructions with the PLC-3 processor use one binary file in a data table section for module location and other related data. This is the block transfer control file. The block transfer data file stores data that you want transferred to the module (when programming a block transfer write) or from the module (when programming a block transfer read). The address of the block transfer data files are stored in the block transfer control file.

The industrial terminal prompts you to create a control file when a block transfer instruction is being programmed. **The same block transfer control file is used for both the read and write instructions for your module.** A different block transfer control file is required for every module.

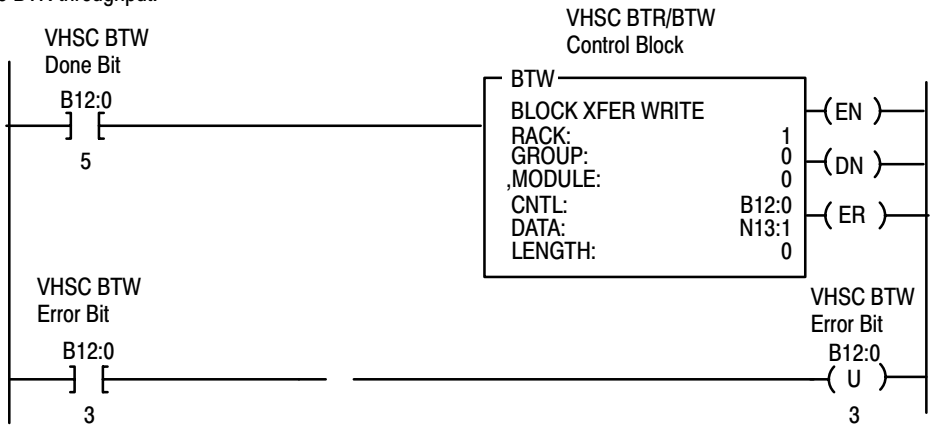
A sample program is shown in Figure 3.2 below.

Figure 3.2
PLC-3 Family Sample Program Structure

The VHSC module is located in rack 1, module group 0, slot 0. The control file is a 10 word file, shared by the BTR and BTW, starting at B12:0. The data obtained by the processor from the VHSC is placed in memory starting at location N13:101, and with the default length of 0 is 18 words long. The MSD of counter 0 is stored in N13:103 and the LSD of counter 0 is stored in N13:104.



The VHSC module is located in rack 1, module group 0, slot 0. The control file is a 10 word file, shared by the BTR and BTW, starting at B12:0. The data sent by the processor to the VHSC is placed in memory starting at location N13:1, and with the default length of 0 is 64 words long. If the default mode of VHSC operation is desired (rollover at 999,999 outputs disabled), this rung can be optional. The module configured bit can also be used as a precondition to increase BTR throughput.



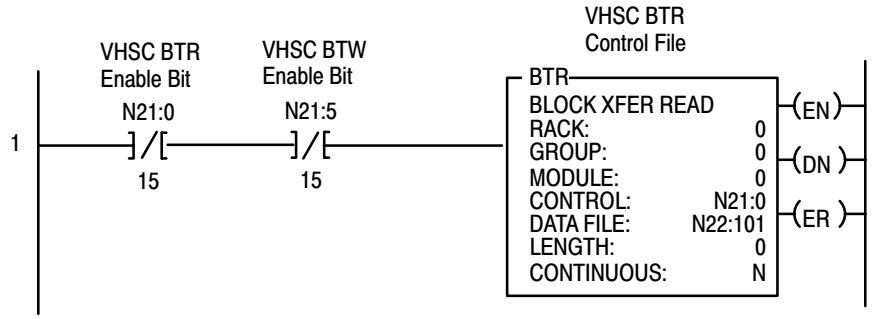
PLC-5 Program Example

Block transfer instructions with the PLC-5 processor use one binary file in a data table section for module location and other related data. This is the block transfer control file. The block transfer data file stores data that you want transferred to the module (when programming a block transfer write) or from the module (when programming a block transfer read). The address of the block transfer data files are stored in the block transfer control file.

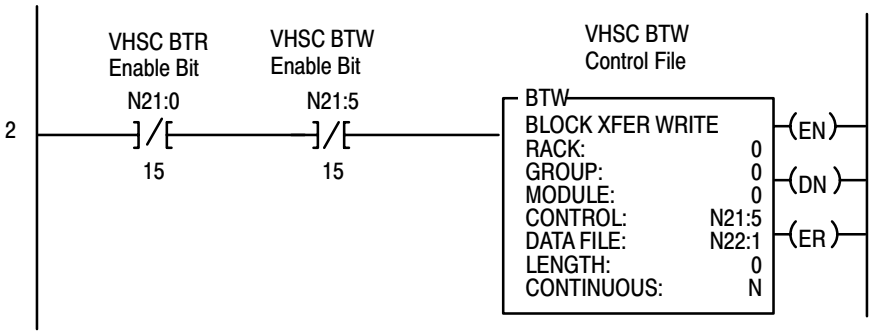
The industrial terminal prompts you to create a control file when a block transfer instruction is being programmed. **A different block transfer control file is used for the read and write instructions for your module.**

Figure 3.3
PLC-5 Family Sample Program Structure

The VHSC module is located in rack 0, module group 0, slot 0. The BTR control file starts at N21:0 and is 5 words long. The data obtained by the processor from the VHSC is placed in memory starting at location N22:101, and with the default length of 0 is 18 words long. The MSD of counter 0 is stored in N22:103 and the LSD of counter 0 is stored in N22:104.



The VHSC module is located in rack 0, module group 0, slot 0. The BTWcontrol file starts at N21:5 and is a 5 words long.
The data sent by the processor to the VHSC is stored in memory starting at location N22:1, and with the default length of 0 is 64 words long.



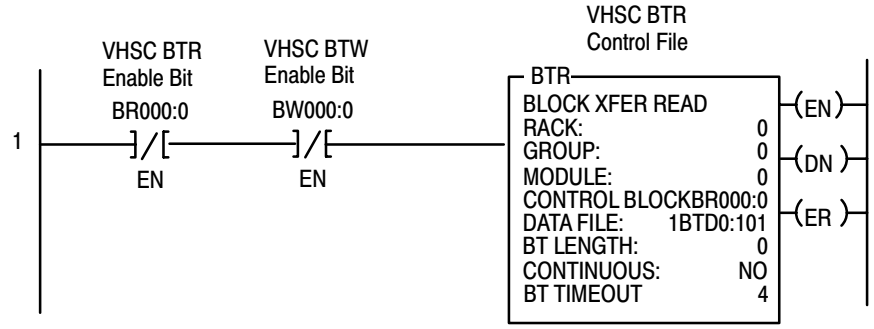
PLC-5/250 Program Example

Block transfer instructions with the PLC-5/250 processor use one binary file in a data table section for module location and other related data. This is the block transfer control file. The block transfer data file stores data that you want transferred to the module (when programming a block transfer write) or from the module (when programming a block transfer read). The address of the block transfer data files are stored in the block transfer control file.

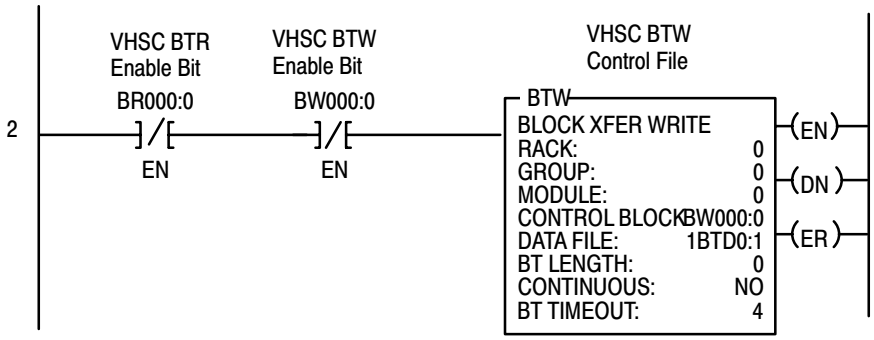
The industrial terminal will automatically select the control file based on rack, group, and slot, and whether it is a read or write. **A different block transfer control file is used for the read and write instructions for your module.** A different block transfer control file is required for every module.

Figure 3.4
PLC-5/250 Family Sample Program Structure

The VHSC module is located in rack 0, module group 0, slot 0. The data obtained by the processor from the VHSC is placed in memory starting at location 1BTD0:101, and with the default length of 0 is 18 words long. The MSD of counter 0 is stored in 1BTD0:103 and the LSD of counter 0 is stored in 1BTD0:104.



The VHSC module is located in rack 0, module group 0, slot 0. The data sent by the processor to the VHSC is stored in memory starting at location 1BTD0:1, and with the default length of 0 is 64 words long.



Chapter Summary

In this chapter, you learned how to program your programmable controller and you were given sample programs for each family of controllers. For additional programs, refer to Appendix B.

Configuring Your Module

Chapter Objectives

In this chapter you will read how to configure your module's hardware, condition your inputs and enter your data.

Configuring the VHSC Module

You must configure your module to conform to the input device and specific application that you have chosen. Data is conditioned through a group of data table words that are transferred to the module using a block transfer write (BTW) instruction.

You can configure the following features for the 1771-VHSC module:

- type of input
- data format
- preset values
- rollover values

Configure your module for its intended operation by means of your programming terminal and write block transfers.

Note: Programmable controllers that use 6200 software (release 4.2 or higher) programming tools can take advantage of the IOCONFIG Addendum utility to configure this module. IOCONFIG Addendum uses menu–based screens for configuration without having to set individual bits in particular locations. Refer to your 6200 software literature for details.

Important: It is strongly recommended that you use IOCONFIG Addendum to configure this module. The IOCONFIG Addendum utility greatly simplifies configuration. If the IOCONFIG Addendum is not available, you must enter data directly into the data table. Use this chapter as a reference when performing this task.

During normal operation, the processor transfers from 1 to 64 words to the module when you program a BTW instruction to the module's address.

Configuration Block for a Block Transfer Write

The complete configuration block for the block transfer write to the module is defined in Table 4.A below.

Table 4.A
Configuration Block for the VHSC Module Block Transfer Write

Word	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	Format				Preset				New Data Acknowledge				Reset			
2	Force Outputs								Enable Outputs							
3	Gate/ Reset	Counter 1 configuration							Gate/ Reset	Counter 0 configuration						
4	Gate/ Reset	Counter 3 configuration							Gate/ Reset	Counter 2 configuration						
5	Rollover Counter 0 MSD															
6	Rollover Counter 0 LSD															
7	Rollover Counter 1 MSD															
8	Rollover Counter 1 LSD															
9	Rollover Counter 2 MSD															
10	Rollover Counter 2 LSD															
11	Rollover Counter 3 MSD															
12	Rollover Counter 3 LSD															
13	Preset Counter 0 MSD															
14	Preset Counter 0 LSD															
15	Preset Counter 1 MSD															
16	Preset Counter 1 LSD															
17	Preset Counter 2 MSD															
18	Preset Counter 2 LSD															
19	Preset Counter 3 MSD															
20	Preset Counter 3 LSD															
21	Scaler 1, Counter 0															
22	Scaler 2, Counter 1															
23	Scaler 3, Counter 2															
24	Scaler 4, Counter 3															
25	Not used												Tie Output 0 to Counter			
26	Output 0 On MSD															
27	Output 0 On LSD															
28	Output 0 Off MSD															
29	Output 0 Off LSD															
30	Not used												Tie Output 1 to Counter			
31	Output 1 On MSD															
32	Output 1 On LSD															
33	Output 1 Off MSD															

Word	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
34	Output 1 Off LSD															
Words repeat for each additional output: 35-39 output 2, 40-44 output 3, 45-49 output 4, 50-54 output 5, 55-59 output 6																
60	Not used												Tie Output 7 to Counter			
61	Output 7 On MSD															
62	Output 7 On LSD															
63	Output 7 Off MSD															
64	Output 7 Off LSD															

Bit/Word Descriptions

Bit/word descriptions of BTW file words are presented in Table 4.B. Enter data into the BTW instruction after entering the instruction into your ladder diagram program.

Table 4.B
Bit/Word Definitions for the VHSC Module

Word	Bits	Description
Word 1	bits 00-03	These bits control the reset function. When one of these bits transitions from 0 to 1, the counter is reset to 0 and begins counting. The bits correspond to the 4 counters: bit 00 = counter 0; bit 01 = counter 1; bit 02 = counter 2; bit 03 = counter 3.
	bits 04-07	New data acknowledge bits. When one of these bits transitions from 0 to 1 the corresponding new data bit in BTR word 1, bits 4-7 will be reset. Bit 04 corresponds to counter 0, bit 05 to counter 1, etc.
	bits 08-11	These bits control the preset function. When one of these bits is set to 1, the preset count value is automatically loaded into the counter and the counter begins counting. (Note: The preset count values are loaded into words 13 through 20.) The bits correspond to the counters as follows: Bit 08 = counter 0; bit 09 = counter 1; bit 10 = counter 2; bit 11 = counter 3.
	bits 12-14	Not used
	bit 15	This bit determines whether BCD or binary format is used. Bit 15 = 0 Indicates all values in the BTW file and the BTR file will be in binary. (Diagnostic byte (word 1) is always BCD.) Bit 15 = 1 Indicates all values in the BTW file and the BTR file will be in BCD.
Word 2	bits 00-07	Enables outputs. Bit 00 corresponds to output 0, bit 01 to output 1, etc. Outputs must be enabled before they can be turned ON. Bits must be set (1) before the output can be turned on.
	bits 08-15	Output forcing bits. Setting a bit to 1 allows the output to be forced. Bit 08 corresponds to output 0, bit 09 corresponds to output 1, etc. Outputs must also be enabled.

Word	Bits	Description
Word 3	bits 00-02	Determine rate measurement mode, encoder mode, counter mode or period/rate mode for **COUNTER 0.**

Mode	Bit	02	01	00
Counter mode		0	0	0
Encoder X1 mode		0	0	1
Encoder X4 mode		0	1	0
Counter not used		0	1	1
Period/rate mode		1	0	0
Rate Measurement mode		1	0	1
Continuous/rate mode		1	1	0

bit 03	Not used
bits 04-06	Determine store count mode for **COUNTER 0**.

Mode	Bit	06	05	04
Store count mode not used for counter 0		0	0	0
Mode 1 (store/continue) used		0	0	1
Mode 2 (store/wait/resume) used		0	1	0
Mode 3 (store-reset/wait/start) used		0	1	1
Mode 4 (store-reset/start) used		1	0	0

bit 07	Invert signal bit for gate/reset terminal. 0 = Not inverted 1 = Inverted
bits 08-10	Determine rate measurement mode, encoder mode, counter mode or period/rate mode for **COUNTER 1.**

Mode	Bit	10	09	08
Counter mode		0	0	0
Encoder X1 mode		0	0	1
Encoder X4 mode		0	1	0
Counter not used		0	1	1
Period/rate mode		1	0	0
Rate Measurement mode		1	0	1
Continuous/rate mode		1	1	0

bit 11	Not used
bits 12-14	Determine store count mode for **COUNTER 1**.

Mode	Bit	14	13	12
Store count mode not used for counter 1		0	0	0
Mode 1 (store/continue) used		0	0	1
Mode 2 (store/wait/resume) used		0	1	0
Mode 3 (store-reset/wait/start) used		0	1	1
Mode 4 (store-reset/start) used		1	0	0

<table>
<tr><th>Word</th><th>Bits</th><th>Description</th></tr>
<tr><td></td><td>bit 15</td><td>Invert signal bit for gate/reset terminal.
0 = Not inverted
1 = Inverted</td></tr>
<tr><td>Word 4</td><td>bits 00-02</td><td>Determine rate measurement mode, encoder mode, counter mode or period/rate mode for COUNTER 2.
<table>
<tr><th>Mode</th><th>Bit</th><th>02</th><th>01</th><th>00</th></tr>
<tr><td>Counter mode</td><td></td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Encoder X1 mode</td><td></td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Encoder X4 mode</td><td></td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Counter not used</td><td></td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Period/rate mode</td><td></td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Rate Measurement mode</td><td></td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>Continuous/rate mode</td><td></td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td></td><td>bit 03</td><td>Not used</td></tr>
<tr><td></td><td>bits 04-06</td><td>Determine store count mode for COUNTER 2.
<table>
<tr><th>Mode</th><th>Bit</th><th>06</th><th>05</th><th>04</th></tr>
<tr><td>Store count mode not used for counter 2</td><td></td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Mode 1 (store/continue) used</td><td></td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Mode 2 (store/wait/resume) used</td><td></td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Mode 3 (store-reset/wait/start) used</td><td></td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Mode 4 (store-reset/start) used</td><td></td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td></td><td>bit 07</td><td>Invert signal bit for gate/reset terminal.
0 = Not inverted
1 = Inverted</td></tr>
<tr><td></td><td>bits 08-10</td><td>Determine rate measurement mode, encoder mode, counter mode or period/rate mode for COUNTER 3.
<table>
<tr><th>Mode</th><th>Bit</th><th>10</th><th>09</th><th>08</th></tr>
<tr><td>Counter mode</td><td></td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Encoder X1 mode</td><td></td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Encoder X4 mode</td><td></td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Counter not used</td><td></td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Period/rate mode</td><td></td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Rate Measurement mode</td><td></td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>Continuous/rate mode</td><td></td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td></td><td>bit 11</td><td>Not used</td></tr>
<tr><td></td><td>bits 12-14</td><td>Determine store count mode for COUNTER 3.
<table>
<tr><th>Mode</th><th>Bit</th><th>14</th><th>13</th><th>12</th></tr>
<tr><td>Store count mode not used for counter 3</td><td></td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Mode 1 (store/continue) used</td><td></td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Mode 2 (store/wait/resume) used</td><td></td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Mode 3 (store-reset/wait/start) used</td><td></td><td>0</td><td>1</td><td>1</td></tr>
</table></td></tr>
</table>

Word	Bits	Description			
		Mode 4 (store-reset/start) used	1	0	0
	bit 15	Invert signal bit for gate/reset terminal. 0 = Not inverted 1 = Inverted			
Words 5 thru 12		Rollover value. When rollover value is reached, the counter value becomes 000,000 and counting continues from that point. The range for both MSD and LSD is 0 to 999.			
Word 5		Rollover value. Most significant digit for counter 0.			
Word 6		Rollover value. Least significant digit for counter 0.			
Word 7		Rollover value. Most significant digit for counter 1.			
Word 8		Rollover value. Least significant digit for counter 1.			
Word 9		Rollover value. Most significant digit for counter 2.			
Word 10		Rollover value. Least significant digit for counter 2.			
Word 11		Rollover value. Most significant digit for counter 3.			
Word 12		Rollover value. Least significant digit for counter 3.			
Words 13 thru 20		Preset values. The preset value is loaded into the respective counter when its preset bit is set. The preset count value overrides the current count, and becomes the new count value in the counter. When a preset value is loaded, the counter begins to count from that value.			
Word 13		Preset value. Most significant digit for counter 0.			
Word 14		Preset value. Least significant digit for counter 0.			
Word 15		Preset value. Most significant digit for counter 1.			
Word 16		Preset value. Least significant digit for counter 1.			
Word 17		Preset value. Most significant digit for counter 2.			
Word 18		Preset value. Least significant digit for counter 2.			
Word 19		Preset value. Most significant digit for counter 3.			
Word 20		Preset value. Least significant digit for counter 3.			
Words 21 thru 24		The ranges of words 21 thru 24 depend on the mode selected in word 3, bits 00-02. In encoder/counter mode or period/rate mode, these are scalar words, and divide the incoming pulse train at the gate/reset terminal by a predetermined integer (1, 2, 4, 8, 16, 32, 64 and 128). Default value is 1. In rate measurement mode, these are time base values. Range is in milliseconds from 10ms to 2 seconds in 10ms intervals.			
Word 25	bits 00-03	Allows you to tie the output to any of the 4 counters. Bits correspond to the counters: bit 00 for counter 0, bit 01 for counter 1, bit 02 for counter 2, and bit 03 for counter 3.			
	bits 04-15	Not used.			
Word 26		Most significant digit of the ON value of output 0.			
Word 27		Least significant digit of the ON value of output 0.			
Word 28		Most significant digit of the OFF value of output 0.			
Word 29		Least significant digit of the OFF value of output 0.			
Words 30 thru 34		These words are a repeat of words 25 through 29 with the exception of the output number. These words are for output 1.			

Word	Bits	Description
Words 35 thru 39		These words are a repeat of words 25 through 29 with the exception of the output number. These words are for output 2.
Words 40 thru 44		These words are a repeat of words 25 through 29 with the exception of the output number. These words are for output 3.
Words 45 thru 49		These words are a repeat of words 25 through 29 with the exception of the output number. These words are for output 4.
Words 50 thru 54		These words are a repeat of words 25 through 29 with the exception of the output number. These words are for output 5.
Words 55 thru 59		These words are a repeat of words 25 through 29 with the exception of the output number. These words are for output 6.
Words 60 thru 64		These words are a repeat of words 25 through 29 with the exception of the output number. These words are for output 7.

Chapter Summary

In this chapter you learned how to configure your module's hardware, condition your inputs and enter your data.

Module Status and Input Data

Chapter Objectives

In this chapter you will read about:

- reading data from your module
- module read block transfer format

Reading Data from the Module

Block transfer read (BTR) programming moves status and data from the input module to the processor's data table (Table 5.A). The processor user program initiates the request to transfer data from the module to the processor.

Block Transfer Read for the 1771-VHSC Module

The module transfers up to 26 words to the processor's data table file. The words contain module status and input data from each channel. When a BTR of length 0 is programmed, the module returns 18 words.

Important: Words 19 through 26 are optional, and are accessed only by programming a BTR length greater than 18 words. Words 19 through 26 are only valid if in period/rate or continuous/rate modes. In any other mode words 19 through 26 are zero.

Table 5.A
BTR Word Assignments for the VHSC Module (1771-VHSC)

(Octal Bit)	17	16	15	14	13	12	11	10	07	06	05	04	03	02	01	00
Decimal Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
1	Diagnostics (always in BCD)								New Data				Not Used			PU*
2	Not used				Gate/Reset input state				Status of outputs							
3	Counter 0 MSD (0-999)															
4	Counter 0 LSD (0-999)															
5	Counter 1 MSD (0-999)															
6	Counter 1 LSD (0-999)															
7	Counter 2 MSD (0-999)															
8	Counter 2 LSD (0-999)															
9	Counter 3 MSD (0-999)															
10	Counter 3 LSD (0-999)															
11	Counter 0 Store count values MSD (range 0-999) in encoder/counter mode; or frequency value MSD (range 0-500) in rate measurement or period/rate mode															
12	Counter 0 Store count values LSD (range 0-999)															

(Octal Bit)	17	16	15	14	13	12	11	10	07	06	05	04	03	02	01	00
Decimal Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
13	Counter 1 Store count values MSD (range 0-999) in encoder/counter mode; or frequency value MSD (range 0-500) in rate measurement or period/rate mode															
14	Counter 1 Store count values LSD (range 0-999)															
15	Counter 2 Store count values MSD (range 0-999) in encoder/counter mode; or frequency value MSD (range 0-500) in rate measurement or period/rate mode															
16	Counter 2 Store count values LSD (range 0-999)															
17	Counter 3 Store count values MSD (range 0-999) in encoder/counter mode; or frequency value MSD (range 0-500) in rate measurement or period/rate mode															
18	Counter 3 Store count values LSD (range 0-999)															
19	Counter 0 Total counts occurring at gate/reset pin in period/rate or continuous/rate modes (MSD range = 0-999)															
20	Counter 0 Total counts occurring at gate/reset pin in period/rate or continuous/rate modes (LSD range = 0-999)															
21	Counter 1 Total counts occurring at gate/reset pin in period/rate or continuous/rate modes (MSD range = 0-999)															
22	Counter 1 Total counts occurring at gate/reset pin in period/rate or continuous/rate modes (LSD range = 0-999)															
23	Counter 2 Total counts occurring at gate/reset pin in period/rate or continuous/rate modes (MSD range = 0-999)															
24	Counter 2 Total counts occurring at gate/reset pin in period/rate or continuous/rate modes (LSD range = 0-999)															
25	Counter 3 Total counts occurring at gate/reset pin in period/rate or continuous/rate modes (MSD range = 0-999)															
26	Counter 3 Total counts occurring at gate/reset pin in period/rate or continuous/rate modes (LSD range = 0-999)															

*** PU** = Power up bit (refer to word/bit description)
Note: Words 19 through 26 are optional and used only in period/rate and continuous/rate modes. They can only be accessed by making the BTR length between 19 and 26.

Bit/Word Description for Block Transfer Read

Table 5.B provides bit/word descriptions for the block transfer read instruction returned by the 1771-VHSC module to the processor.

Table 5.B
Bit/Word Description for the VHSC Module (1771-VHSC)

Word	Bit	Definition
Word 1	Bit 00	Power-up bit indicates whether a successful BTW with valid data has occurred since powerup, or since last switched from Program to Run mode. Bit = 0 - A successful BTW has occurred Bit = 1 - A successful BTW has **not** occurred
	Bits 01-03	Not used
	Bits 04-07	New data bits. Indicates that a store register (BTR words 11-18) has been updated. These bits are reset by a 0 to 1 transition of the new data acknowledge bits in BTW word 1, bits 4-7. Bit 04 corresponds to counter 0, bit 05 to counter 1, etc.
	Bits 08-15 (Bits 10-17)	Diagnostic byte. Always in BCD. This byte indicates the number of the first word in the BTW file that was incorrect. Refer to chapter 7 for other diagnostic error codes returned by the module.
Word 2	Bits 00-07	Status bits for outputs. Bit 00 corresponds to output 0, bit 01 to counter 2, etc. Bit = 0 - output OFF Bit = 1 - output ON
	Bits 08-11 (Bits 10-12)	State of gate/reset input. Bit 08 (10) corresponds to counter 0, bit 09 (11) to counter 1, etc. Bit = 0 - gate input inactive Bit = 1 - gate input active
	Bits 12-15 (Bits 13-17)	Not used
Word 3		Contains the most significant digit for counter 0. The allowable range is 0-999.
Word 4		Contains the least significant digit for counter 0. The allowable range is 0-999.
Word 5		Contains the most significant digit for counter 1. The allowable range is 0-999.
Word 6		Contains the least significant digit for counter 1. The allowable range is 0-999.
Word 7		Contains the most significant digit for counter 2. The allowable range is 0-999.
Word 8		Contains the least significant digit for counter 2. The allowable range is 0-999.
Word 9		Contains the most significant digit for counter 3. The allowable range is 0-999.
Word 10		Contains the least significant digit for counter 3. The allowable range is 0-999.
Words 11		Counter 0 Store count values MSD (range 0-999) in encoder/counter mode; or frequency value MSD (range 0-500) in rate measurement or period/rate mode

Word	Bit	Definition
Words 12		Counter 0 Store count values LSD (range 0-999)
Words 13		Counter 1 Store count values MSD (range 0-999) in encoder/counter mode; or frequency value MSD (range 0-500) in rate measurement or period/rate mode
Words 14		Counter 1 Store count values LSD (range 0-999)
Words 15		Counter 2 Store count values MSD (range 0-999) in encoder/counter mode; or frequency value MSD (range 0-500) in rate measurement or period/rate mode
Words 16		Counter 2 Store count values LSD (range 0-999)
Words 17		Counter 3 Store count values MSD (range 0-999) in encoder/counter mode; or frequency value MSD (range 0-500) in rate measurement or period/rate mode
Words 18		Counter 3 Store count values LSD (range 0-999)
Word 19		Counter 0 Total counts occurring at gate/reset pin in period/rate or continuous/rate modes (MSD range = 0-999)
Word 20		Counter 0 Total counts occurring at gate/reset pin in period/rate or continuous/rate modes (LSD range = 0-999)
Word 21		Same as word 19, but for counter 1.
Word 22		Same as word 20, but for counter 1.
Word 23		Same as word 19, but for counter 2.
Word 24		Same as word 20, but for counter 2.
Word 25		Same as word 19, but for counter 3.
Word 26		Same as word 20, but for counter 3.

Chapter Summary

In this chapter you learned the meaning of the status information that the module sends to the processor.

Troubleshooting

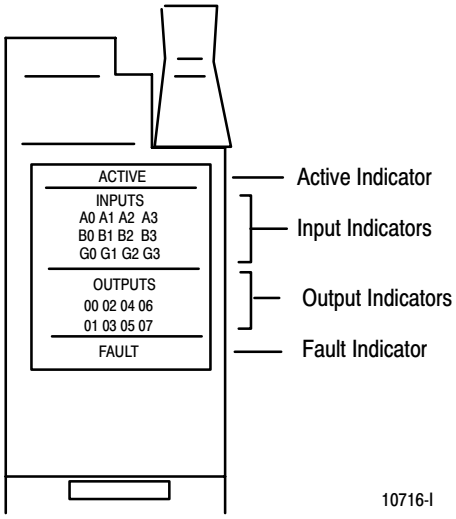
Chapter Objectives

In this chapter you will learn how to troubleshoot your VHSC module using the indicators on the front of the module, and the troubleshooting flowchart.

Using the Indicators for Troubleshooting

The indicators on the front of the module are an aid in troubleshooting. These indicators consist of:

- active indicator
- input indicators
- output indicators
- fault indicator



The active indicator is on when the module has successfully powered up. When an input indicator (A, B) is on, it indicates that the input is high. When the output indicator is on, it indicates that the module has commanded the output to be on. When a gate/reset indicator (G) is on, its input is high. Since that signal can be inverted, it does not indicate whether the signal on that terminal is necessarily logically true.

A troubleshooting chart is shown below.

Troubleshooting Chart

Indication	Probable Cause	Corrective Action
Active LED ON	The module has successfully powered up.	Normal. No action required.
Active OFF	The module has not powered up successfully.	Check fault light, and rack power supply.
Input LED ON	A signal is available at the designated input terminal (high).	Normal. No action required.
Input LED OFF	A signal is not available at the designated input terminal (low).	Normal. No action required.
Fault LED ON	Internal problem.	Power down the module, reseat in I/O chassis, and restore power. If the fault LED remains on, replace module.
Output LED ON	The module has commanded an output on.	Normal. No action required.
Output LED OFF	The output is off.	Normal. No action required.

Diagnostic Codes Returned by the Module

The VHSC module returns diagnostics in word 1 of the block transfer read (BTR) to the processor. These codes are identified below.

Diagnostics Reported in Word 1 of BTR

Word	Bit	Indication	
1	Bit 00	Power-up bit indicates whether a successful BTW with valid data has occurred since power-up, or since last switched from Program to Run mode. Bit 0 = 0 - Successful BTW Bit 0 = 1 - BTW has not occurred	
	Bits 01-03	Not used	
	Bits 04-07	New data bits. Bit 04 corresponds to counter 0, bit 05 to counter 1, etc.	
	Bits 08-15	Diagnostic byte. This byte is always in BCD format. This byte indicates which word (1-64) in the BTW file that was incorrect, or one of the following error codes. The codes are as follows:	
		Code	
		87	Preset or reset illegal for counter 0 with frequency mode
		88	Preset or reset illegal for counter 1 with frequency mode
		89	Preset or reset illegal for counter 2 with frequency mode
		90	Preset or reset illegal for counter 3 with frequency mode
		91	Store count illegal for counter 0 with frequency mode
		92	Store count illegal for counter 1 with frequency mode
		93	Store count illegal for counter 2 with frequency mode
		94	Store count illegal for counter 3 with frequency mode
		95	Preset greater than rollover for counter 0
		96	Preset greater than rollover for counter 1
		97	Preset greater than rollover for counter 2
		98	Preset greater than rollover for counter 3
		99	BTW length invalid - length not equal to 0, 1, 2, 4, 12, 20, 24, 29, 34, 39, 44, 49, 54, 59, 64.

Chapter Summary

In this chapter, you learned how to interpret the module indicators, and the meanimg of the error codes returned by the module.

Specifications

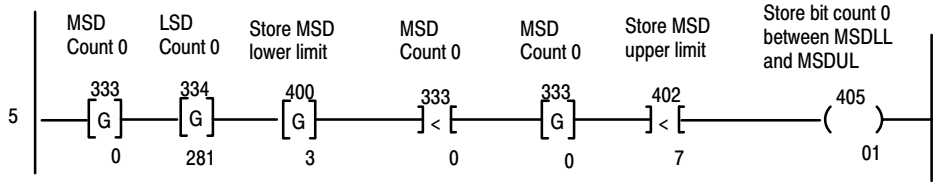
Number of Counters		4
Module Location		1771 Series A or B I/O chassis
Maximum Count Value		0–999,999 (programmable)
BTW Processing Time (worst case)		5.5ms - binary 11ms - BCD } on a configuration change (1.5-2.9ms — typical)
Maximum Input Frequency		100Hz for switch bounce; electromechanical switch (user-selectable) 250kHz in encoder modes (2–channel quadrature) 500kHz in period/rate, rate/measurement and continuous/rate modes 1MHz in counter modes (single channel)
Inputs per Counter		3 – A, B, Gate/reset
Input Voltage		5V or 12–24V (user selectable)
Input Current		Typically 7mA @ 5V; 7.0 to 15.0mA @ 12–24V
Minimum Input Current		4mA
Number of Outputs		8
Maximum Output Off-state Leakage Current		less than 10μA @ 24V dc
Maximum On-state Voltage Drop		0.05Ω x current
Output Control		Any number of outputs are assignable to any of 4 counter channels. One “turn–on” preset value and one “turn–off” preset per output.
Output Voltage		5 to 24V dc, customer supplied
Output Current		2A per channel sourced out of module. All outputs can be on simultaneously without derating.
Output Switching Time		< 10μs turn on; < 100μs turn off Typical: 3μs turn on; 30μs turn off
Filtering		Selectable — high-speed or normal (normal = below 100Hz)
Backplane Current		650mA
Isolation Voltage		1500V between input and backplane 1500V between output and backplane 300V between isolated channels
Power Dissipation		13 Watts (max); 2 Watts (min)
Thermal Dissipation		54.2 BTU/hr (max); 6.8 BTU/hr (min)
Input Conductors	Wire Size Category Length	Belden 9182 or equivalent Category 2[1] 250 feet (76.2m)
Output Conductors	Wire Size Category	14 gauge stranded (max.) 3/64 inch insulation (max.) Category 1[1]
Fuse		2AG 3A fuse — Littelfuse 225003
Environmental Conditions	Operating Temperature Storage Temperature Relative Humidity	0 to 60°C (32 to 140°F) –40 to 85°C (–40 to 185°F) 5 to 95% (without condensation)
Keying		Between 24 and 26 Between 28 and 30
Field Wiring Arm		40-terminal cat. no. 1771–WN
Wiring Arm Screw Torque		7-9 inch-pounds

[1] Use this conductor-category information for planning conductor routing as described in the system-level installation manual.

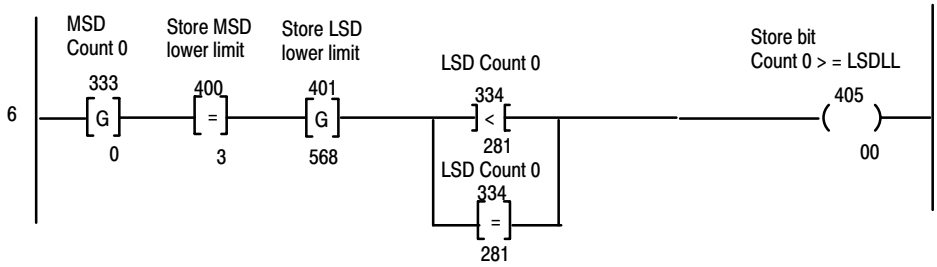
Sample Programs

Sample Program for PLC–2 Family Processors

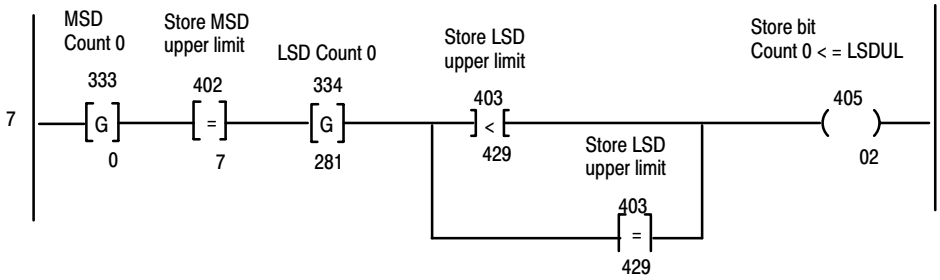
These rungs illustrate a method of monitoring the count for values greater than 3 digits. The total count is displayed in words 333 and 334.
This rung set storage bit 405/1 when the count is between the MSD lower limit and the MSD upper limit.
(MSDLL) < Count 0 < (MSDUL)



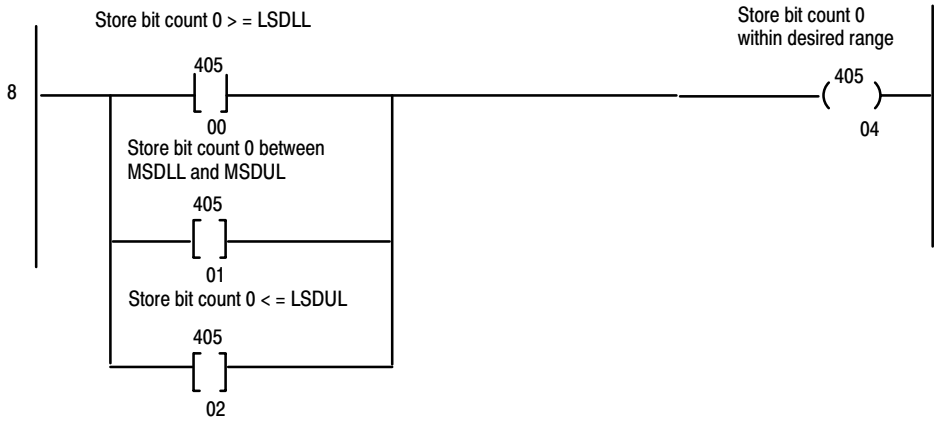
When counting up, this rung will go true first. Bit 405/00 will be set when count 0 is equal to the MSDLL and greater than or equal to the LSDLL. (Count 0 = MSDLL) + (LSDLL < = Count 0)



When counting up, this rung will go true last. Bit 405/02 will be set when count 0 is equal to the MSDUL and less than or equal to the LSDUL. (Count 0 = MSDUL) + (Count 0 < = LSDUL)

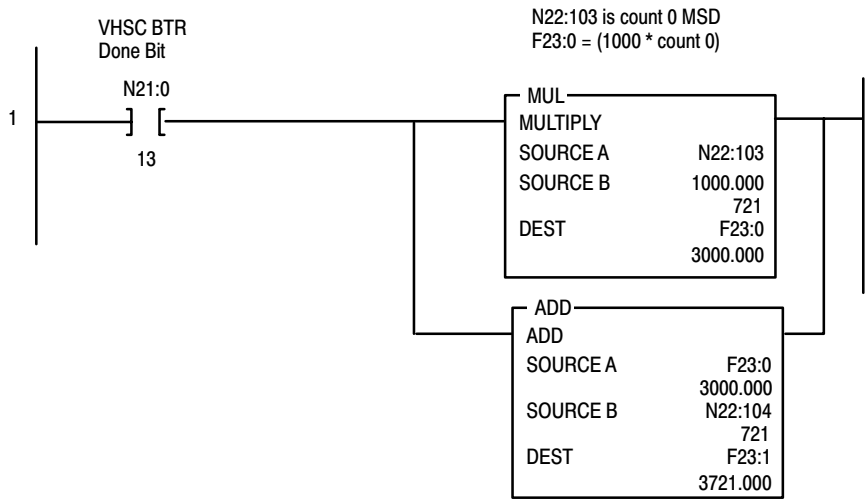


When using all 3 storage bits, bit 405/4 represents when count 0 is within the specified range. In this particular case, when the count is between 3,568 and 7,429

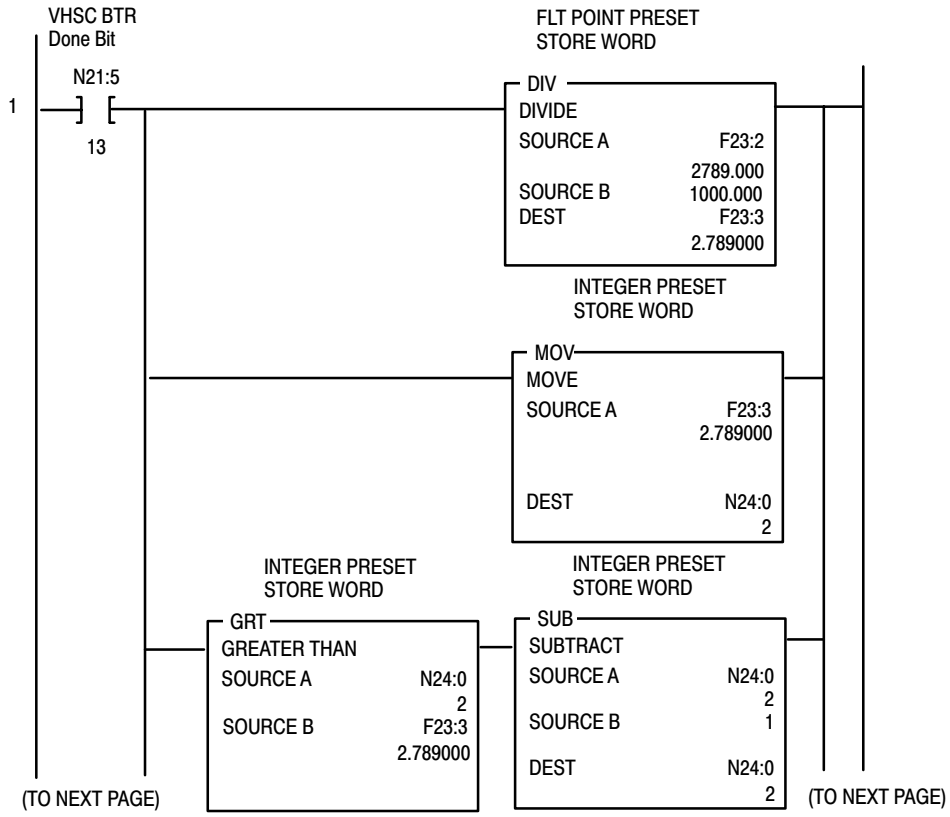


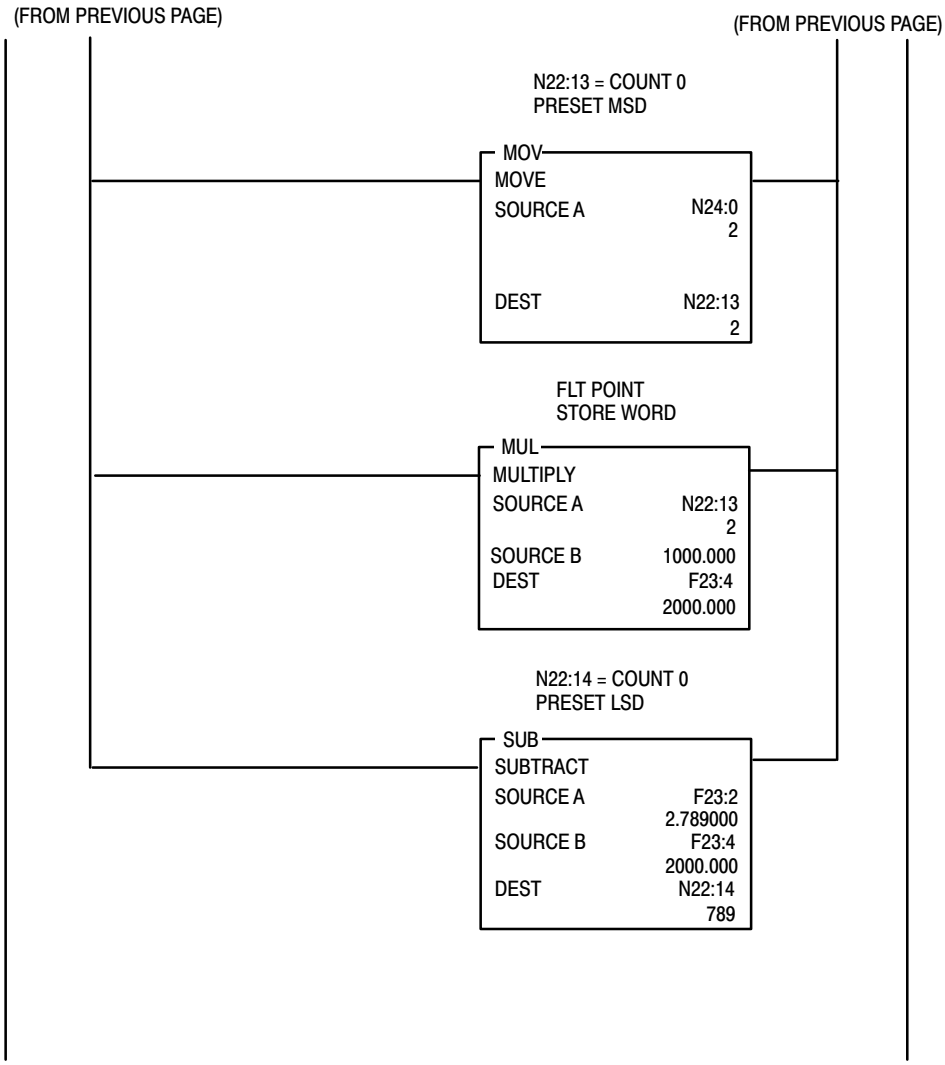
Sample Program for PLC–5 Family Processors

This rung illustrates how to assemble the count MSD and LSD into one floating point word that can be used throughout the program. F23:0 is an intermediate storage value and F23:1 contains the total count 0 value.
Total count = (MSD * 1000) + LSD, [F23:1 = (N22:103 * 1000) + N22:104]

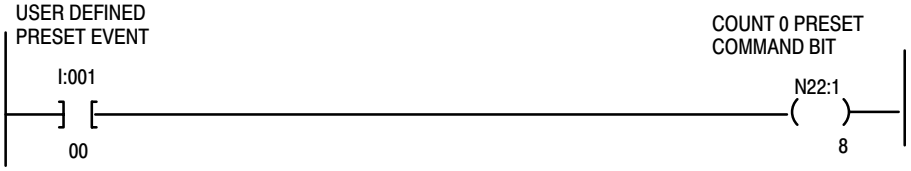


This rung illustrates how to disassemable 1 floating point word into 2 integer words that are used as the MSD and LSD for preset count 0. This same technique can be used for the rollover value as well as the output values.
MSD = TRUNCATE (FLTPNT/1000), [N22:13 = TRUNCATE (F23:2/1000)] while LSD = FLTPNT – (MSD*1000), [N22:14 = F23:2 – (N22:13*1000]



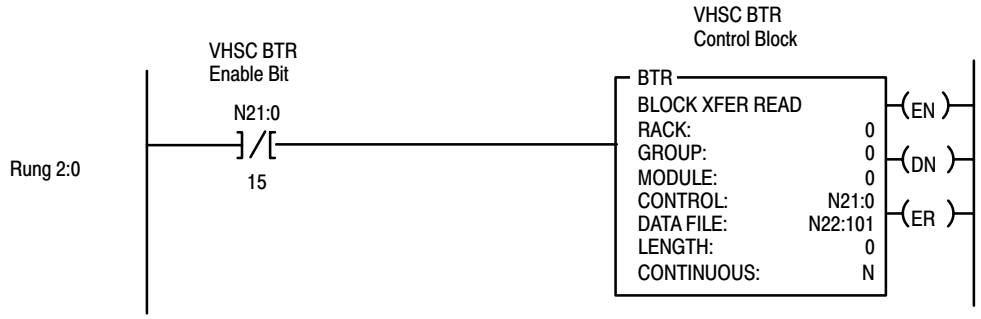


When the module receives a valid BTW with N22:1/8 going from 0 to 1, it will force the count 0 value returned via the BTR in words N22:103 and N22:104 to the BTW value contained in preset 0 words N22:113 and N22:114.

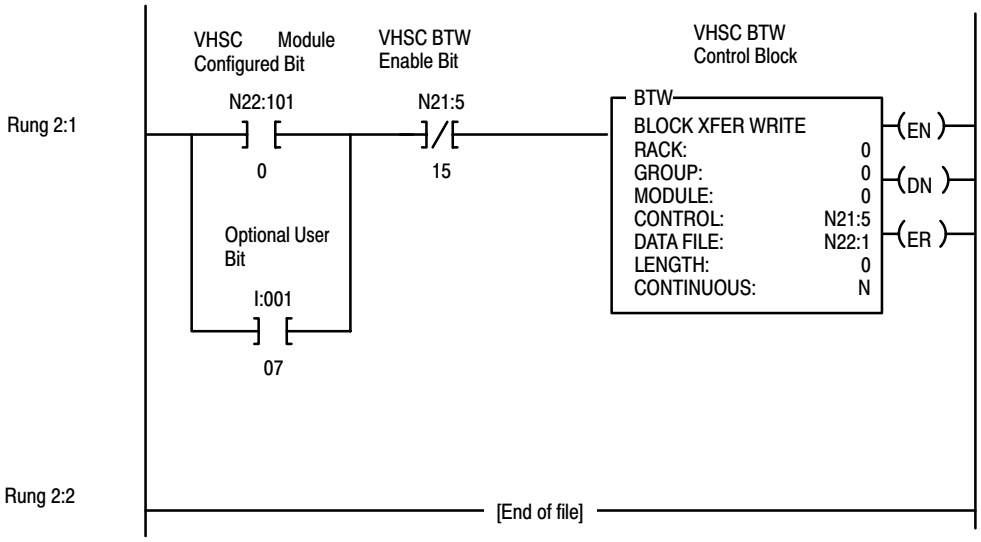


Addditional Sample Program for PLC–5 Family Processors

This block transfer read rung can be used alone or with the block transfer write rung shown below. If used alone, all VHSC counters will operate in a default mode of outputs disabled, rollover at 999,999 and count mode with pulses counted on channel A, direction sensed at channel B and the gate is not active.



If the default module operation is acceptable, this rung can be optional. If it is necessary to reconfigure, this rung will automatically send a new configuration to the module (using the module configured bit N22:101/0 in the BTR file). This will occur on power up and each time the processor is changed from program to run mode. The optional user bit I:001/07 can also configure the module at any time. Not enabling the BTW can increase throughput of the read.



Application Considerations

Appendix Objectives

This appendix will provide you with background for selecting the appropriate input device for your 1771-VHSC module, explain the output circuit, and provide you with information for selecting the type and length of input cabling.

Types of Input Devices

To turn on an input circuit in the VHSC module, you must source current through the input resistors sufficient to turn on the opto-isolator in the circuit.

If no connection is made to a pair of input terminals, no current will flow through the photodiode of the opto-isolator and that channel will be off. Its corresponding input status indicator will be off.

All 12 inputs are electrically identical.

There are 2 basic classes of driver devices built-in to encoders and other pulse sources: single-ended and differential. A single-ended driver output consists of a signal and a ground reference. A differential driver consists of a pair of totem-pole outputs driven out of phase. One terminal actively sources current while the other sinks, and there is no direct connection to ground.

Differential line drivers provide reliable, high speed communication over long wires. Most differential line drivers are powered by 5V, and are more immune to noise than single-ended drivers at any operating voltage.

Any installation must follow customary good wiring practices: separate conduit for low voltage dc control wiring and any 50/60Hz ac wiring, use of shielded cable, twisted pair cables, etc. Refer to publication 1770-4.1, “Programmable Controller Wiring and Grounding Guidelines” for more information.

Examples for Selecting Input Devices

The following examples will help you in determining the best input type for your particular application. These examples include:

5V differential line driver

single-ended driver

open collector circuit

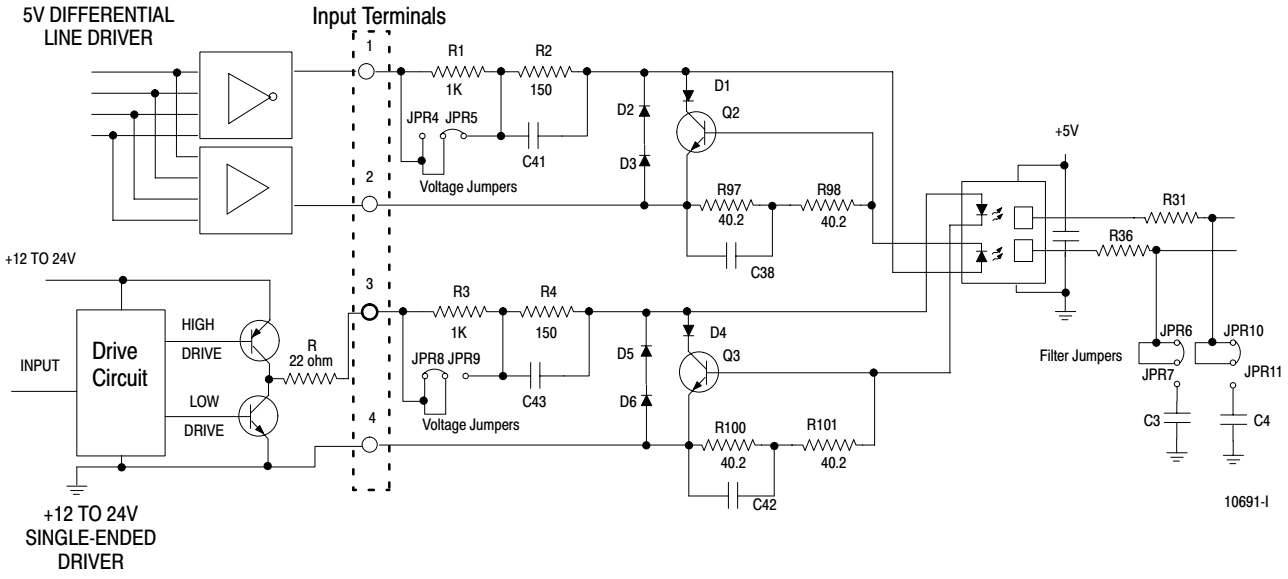
electromechanical limit switch

Circuit Overview

To make sure your signal source and the 1771-VHSC module are compatibility, you need to understand the electrical characteristics of your output driver and its interaction with the 1771-VHSC input circuit.

Refer to Figure C.1. The most basic circuit would consist of R1, R2, JPR4, JPR5, the photodiode and associated circuitry around half of the opto-isolator. The resistors provide first-order current limiting to the photodiodes of the dual high speed opto-isolator. With JPR4 closed, and JPR5 open, the total limiting resistance is R1 + R2 = 1150 ohms. This jumper position is designated "12 to 24 Volt Range." Assuming a 2V drop across the photodiode and R97 and R98, you would have 8.7-19mA demanded from the driving circuit as the applied voltage ranged from 12 to 24V.

Figure C.1
Example Circuits for 5V Differential and +12 to +24V Single-Ended Drivers



In the "5 Volt" position (JPR4 open; JPR5 closed), R1 is shorted and the limiting resistance is 250 ohms. If 5.0V was applied at the input, the current demanded would be (5.0 - 2.0)/150 = 20mA.

The above type of calculation is necessary to the user since the driving device must cause a minimum of 5mA to flow through the photodiode regardless of which jumper position is selected.

The optical isolator manufacturer recommends a maximum of 8mA to flow through the photodiode. This current could be exceeded in the 24V position. To obtain this limit, a dc shunt circuit is included, consisting of D1, Q2, R97 and R98. If the photodiode current exceeds about 8mA, the drop across R97-R98 will be sufficient to turn Q2 on, and any excess current will be shunted through D1 and Q2 instead of through the photodiode.

If the driving device is a standard 5V differential line driver, D2 and D3 provide a path for reverse current when the field wiring arm terminal 1 is logic low and terminal 2 is logic high. The combined drop is about the same at the photodiode (about 1.4V). The circuit appears more symmetrical, or balanced, to the driver as opposed to just one diode.

Detailed Circuit Analysis

In the example above, we used a constant 2.0V drop across the photodiode and R97-R98. To calculate the true photodiode current, consider the photodiode, D1, Q2, R97 and R98 as one circuit. The voltage drop across D1 and Q2 will always be equal to the drop across the photodiode and R97-R98. We will call this V_{drop}.

First, consider the minimum requirement of I_f = 5mA.The V_f curves for this photodiode will typically have a 1.5V drop With 5mA current, R97 and R98 will drop (80.4 ohms x 5mA) = 0.40V. Thus, at 5mA,

$$V_{drop} = (1.5V + 0.40V) = 1.90V.$$

Now let's see what happens when I_f goes to 8mA or above. With the temperature about half way between 25 and 70ºC, V_f becomes about 1.5V. R97-R98 will now drop 0.64V (80.4 ohms x 8mA). That means:

$$V_{drop} = 1.5V + 0.64V = 2.14V.$$

The V_{be} of Q2 is now sufficient to start to turn Q2 on. If the current through the photodiode increases to 9mA, V_{be} becomes 0.72V and Q2 is fully on. Any additional current (supplied by a 24V applied input) will be shunted away from the photodiode and dissipated in Q2 and D1.

Thus, Vdrop will never exceed about 2.52V regardless of the applied voltage. In addition, it will never be less than 1.7V if the minimum of 5mA is flowing. Although there are some minor temperature effects on the photodiode drop, you can expect the value Vdrop to be relatively linear from about 1.9V to 2.14V as the current increases from 5mA to 8mA.

Why is this important? Let's look at the 5V differential line driver example below.

5V Differential Line Driver Example

You want to use a 5V differential line driver in your encoder when you have a long cable run and/or high input frequency or narrow input pulses (input duty cycle < 50%). The top circuit (NO TAG) shows a typical 5V differential line driver. The output is connected to the field wiring arm terminal 1 and is sourcing current and the output to terminal 2 is sinking current. JPR5 is connected to short out resistor R1.

Important: Neither output of the differential line driver can be connected to ground. Damage could occur to your driving device.

To be sure that your device will drive the 1771-VHSC, you must know the electrical characteristics of the output driver component used in your signal source device. The output voltage differential $V_{diff} = (V_{oh} - V_{ol})$ is critical, because this is the drive voltage across the 1771-VHSC input terminals 1 and 2, and the photodiode current is a function of $V_{diff} - V_{drop}$.

The manufacturer of your shaft encoder or other pulse-producing device can provide information on the specific output device used.

Note: Any signal source which uses a standard TTL output device driver rated to source 400µA or less in the high logic state is not compatible with the 1771-VHSC module.

Many popular differential line drivers, such as the 75114, 75ALS192, and the DM8830 have similar characteristics and can source or sink up to 40mA.

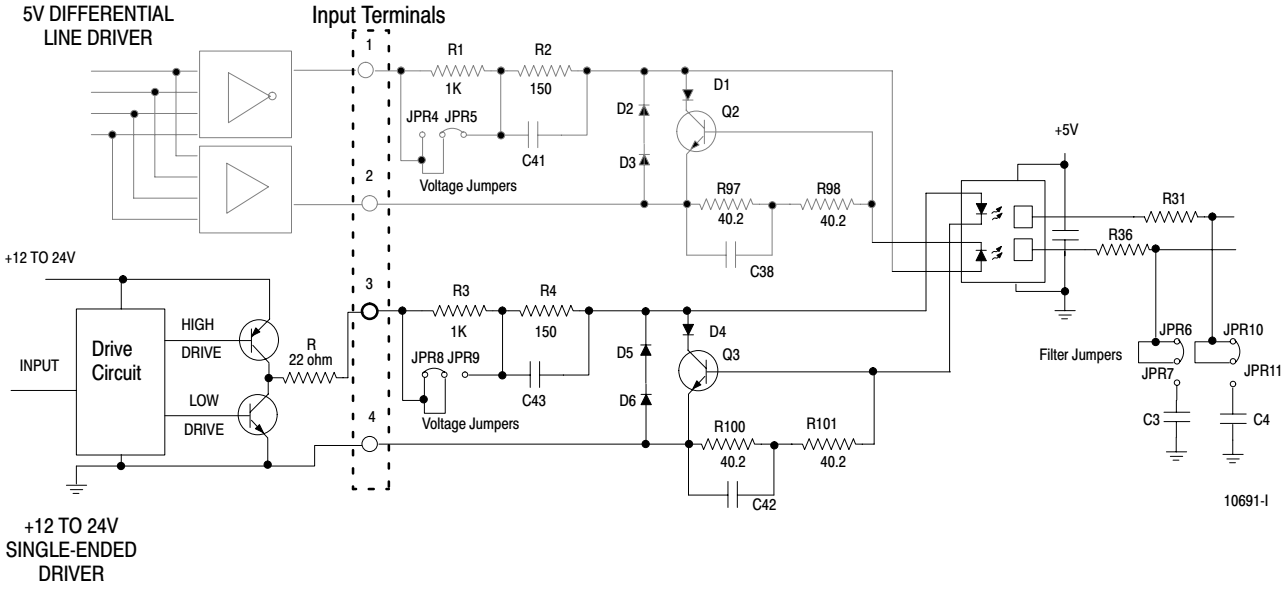
In general, the output voltage V_{oh} will be higher both as the supply voltage and the ambient temperature increase. For example, vendor data for the 75114 shows V_{oh} will be about 3.35V at V_{cc} = 5 V, I_{oh} = 10mA and 25ºC. Vol will be about 0.075V under the same conditions. This means $V_{differential} = V_{oh} - V_{ol}$ = 3.27V if the part is sourcing 10mA. Looking at the curves, if the part were sourcing 5mA you would see V_{diff} = 3.425 - 0.05 = 3.37V.

Assuming that you could supply 5mA to the 1771-VHSC input terminals, how much voltage across the field wiring arm terminals would be required? V_{drop} would be about 1.9V as previously noted. And 5mA through 150 ohms gives an additional 0.75V drop. Thus, you would have to apply about (1.9V + 0.75V) = 2.65V across the terminals to cause a current of 4mA to flow through the photodiode. The 75114 will give about 3.3V at V_{cc} = 5V and 25ºC. Thus you know that this driver will cause more current to flow than the minimum required at 5mA.

+12 to +24V Single-Ended Driver

Some European-made encoders use a circuit similar to the lower circuit in Figure C.2. The current capable of being sourced is limited only by the 22 ohm resistor in the driver output circuit (R). If a 24 volt supply is used, and this driver supplies 15mA, the output voltage would still be about 23V (15mA x 22 ohms = 0.33V, and Vce = .7V).

Figure C.2
Example Circuits for 5V Differential and +12 to +24V Single-Ended Drivers



If the input jumper is in position JPR8, the current to the photodiode is limited by the series resistance of R3 and R4 (about 1.15Kohms). A protection circuit consisting of Q3, R100 and R101 is included. If the current through the photodiode exceeds about 8mA, the voltage across R100 and R101 is sufficient to turn Q3 on, shunting any additional current away from the photodiode. The voltage drop across Q3 will be equal to about 2V (Vphotodiode + Vbe = 2V). The current demanded by the 1771-VHSC input circuit would be about 18mA (23V - 2V/1.15K = 18mA) which is well within the capability of this driver.

Open Collector

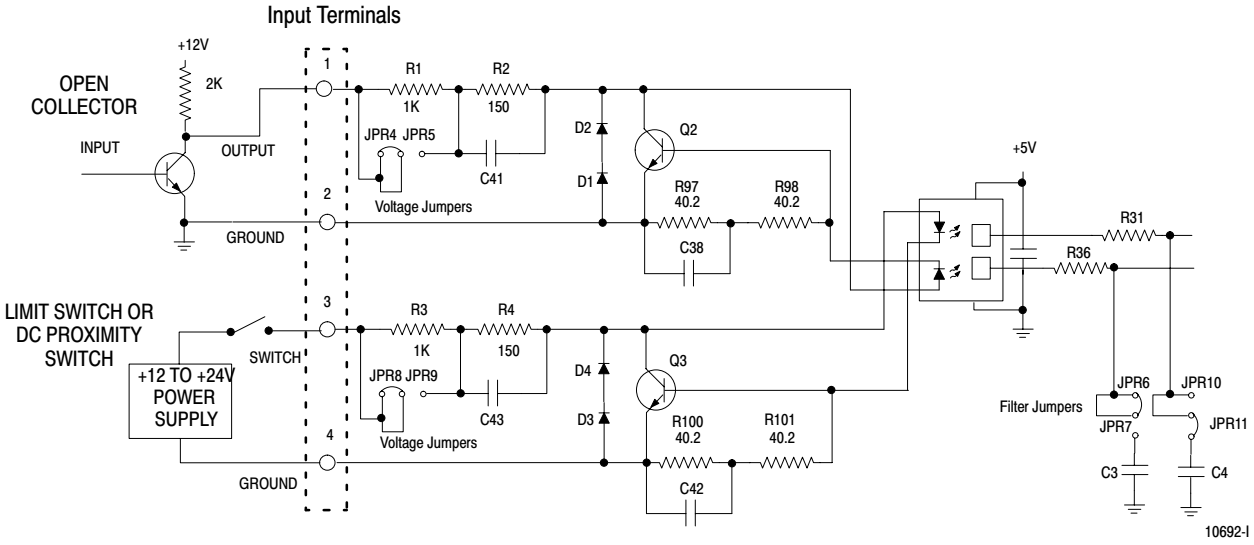
Open collector circuits (the upper circuit in Figure C.3) require close attention so that the input voltage is sufficient to produce the necessary source current, since it is limited not only by the 1771-VHSC input resistors but also the open collector pull-up. Jumper position provides some options as shown in the table below.

Supply Voltage verses Jumper Settings

Supply Voltage	Jumper Setting	Total Impedance	Available Current
+12	JPR4	3.15K	3.2mA (insufficient)
+12	JPR5	2.15K	4.65mA (insufficient)
+24	JPR4	3.15K	7mA (optimal)
+24	JPR5	2.15K	10.2mA (okay)

In this example, you must increase the supply voltage above +12V to make sure there is sufficient input current to overcome the additional 2K source impedance. Note that there is insufficient current with the jumper in the 12-24V position and a +12V supply.

Figure C.3
Example Circuits for Open Collector and Electromechanical Limit Switch



Electromechanical Limit Switch

When using an electromechanical limit switch (the lower circuit in Figure C.3), you must connect the low speed limit capacitor (C4) using jumper JPR11. The RC time constant of R31 and C4 will filter out switch contact bounce. However, this limits the frequency response to around 100Hz. This circuit would be similar when using dc proximity switches, but bounce should not occur unless severe mechanical vibration is present. In either case, source impedance is very low. If you are using a +12 to +24V power supply keep jumper JPR8 in the circuit to add the additional 1K impedance.

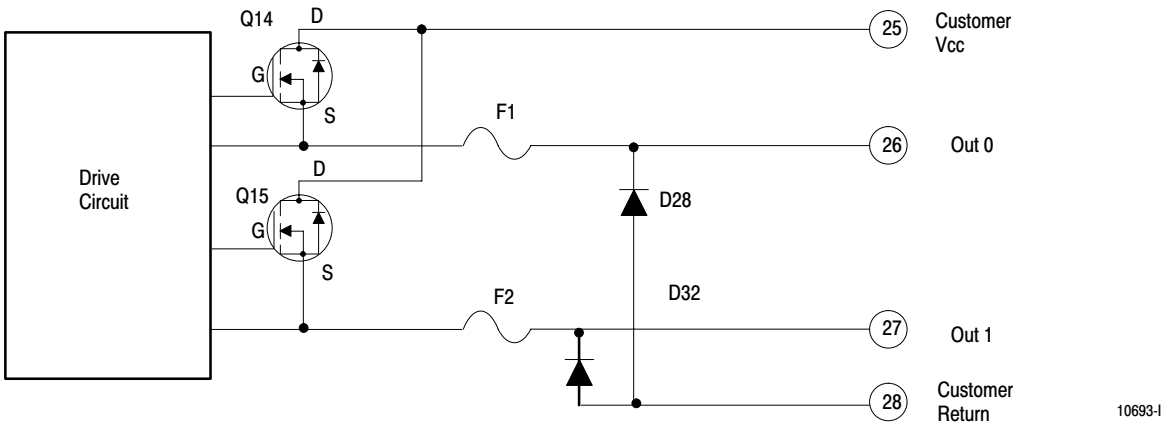
ATTENTION: While the transistor protection circuit limits the optoisolator current to a safe value, make certain that the voltage range jumper JPR9 is not in the circuit. With JPR9 in, you can exceed the 1 Watt dissipation rating on the 150 ohm resistor (R4) and cause permanent damage to the circuit.

Output Circuits

The 1771-VHSC module contains 4 isolated pairs of output circuits. Customer supplied power, ranging from +5V to +24V dc, is connected internally (through terminal Vcc) to the power output transistors. Refer to Figure C.4.When an output is turned on, current flows into the drain, out of the source, through the fuse and into the load connected to the ground of the customer supply (customer return). Diodes D28 and D32 protect the power output transistors from damage due to inductive loads.

If local electrical codes permit, outputs can be connected to sink current. This is done by connecting the load between the power supply + terminal and the customer Vcc terminal on the field wiring arm. The output terminal is then connected directly to ground (customer return). Note that this wiring method **does not** provide inductive load protection for the power output transistors.

Figure C.4
Output Circuit Diagram



Application Considerations

A successful installation depends on the type of input driver, input cable length, input cable impedance, input cable capacitance, frequency of the input.

The following provides information on these installation factors for the 1771-VHSC module.

Input Cable Length

Maximum input cable length depends on the type of output driver in your encoder, the kind of cable used, and maximum frequency at which you will be running. With a differential line driver, 250 feet or less of high quality, low capacitance cable with an effective shield, and an operating frequency of 250KHz or less will likely result in a successfully installation.

If you use an open collector, or other single-ended driver, at distances of 250 feet and frequencies of 250KHz, your chances of success are low. Refer to the table below for suggested desirable driver types.

Desirable	Adequate	Undesirable
5V Line Drivers: such as DM8830, DM88C30, 75ALS192 or equivalent	Balanced Single-Ended: any AC or ACT family part or Discrete, balanced circuit or Open-Collector: suitable for frequencies of < 50KHz	Standard TTL or LSTTL Gates

Totem-pole Output Devices

Standard TTL totem-pole output devices, such as 7404 and 74LS04, are usually rated to source 400 microamps at 2.4V in the high logic state. This is not enough current to turn on a 1771-VHSC input circuit. If your present encoder has this kind of electrical output rating, you cannot use it with the VHSC module.

Most encoder manufacturers, including Allen-Bradley, offer several output options for a given encoder model. When available, choose the high current 5V differential line driver.

Cable Impedance

Generally, you want the cable imedance to match the source and/or load as closely as possible. Using 150 ohm Belden 9182 (or equivalent) cable more closely matches the impedance of both encoder and module input circuits than 78 ohm cable, such as Belden 9463. A closer impedance match minimizes reflections at high frequencies.

Termination of one, or both ends, of the cable with a fixed resistor whose value is equal to the cable impedance will not necessarily improve “reception” at the end of the cable. It will, however, increase the dc load seen by the cable driver.

Cable Capacitance

Use cable with a low capacitance as measured per unit length. High capacitance rounds off incoming square wave edges and takes driver current to charge and discharge. Increasing cable length causes a linear increase in capacitance, which reduces the maximum usable frequency. This is especially true for open collector drivers with resistive pull-ups. For example, Belden 9182 is rated at a very low 9pF/foot.

Cable Length and Frequency

When cable length or frequency goes up, your selection of cable becomes even more critical. Long cables can result in changes in duty cycle, rise and fall times, and phase relationships. The phase relationship between channels A and B in encoder X1 and X4 mode is critical.

The maximum encoder input of 250KHz is designed to work with Allen-Bradley Bulletin 845H or similar incremental encoders with a quadrature specification of 90º (±22º) and a duty cycle specification of 50% (±10%). Any additional phase or duty cycle changes caused by the cable will reduce the specified 250KHz specification.

For any application over 100 feet, and/or over 100KHz, use Belden 9182, a high performance twisted-pair cable with 100% foil shield, a drain wire, moderate 150 ohm inpedance and low capacitance per unit length.

Questions and Answers

General

This appendix presents some of the more commonly asked questions about application and operation of the Very High Speed Counter module.

Questions and Answers

The following questions and answers do not cover all possible questions, but are representative of the more common ones.

Q. If I do not connect channel B in counter mode, what happens to the count status?

A. With channel B disconnected or tied low, the module will count up only. If channel B is tied high, it will count down.

Q. What happens when my processor faults?

A. All outputs will turn off, regardless of the last state switch in the I/O rack.

Q. What happens to my outputs if I place the processor in program mode?

A. All outputs turn off. The inputs will remain active and the module will keep track of count changes. When the processor is returned to RUN mode, the outputs will not become active until after the first valid BTW, and then will be based on the current count.

Q. What does it mean when the indicator for a particular input is on.

A. If the indicator is on, it means that the input is tied high. If the indicator is off, the input is floating or tied low.

Q. What do my indicators mean if I configure the gate input to be inverted?

A. The gate indicator will illuminate when the input is tied high, and turns off when floating or tied low. The gate inversion is seen internally by the module.

Q. What does it mean when an output indicator is on?

A. Since the output indicator is tied to the control side of the module, it means that the module has commanded the output on. It does not necessarily mean that the output is on. The indicator illuminates even when no connection is made to the outputs or to the output supply. For an output to actually turn on, the output supply must be connected.

Q. What are the delay times for turning the outputs on and off?

A. The outputs turn on in $\leq$ 10µsec, and turn off in $\leq$ 100µsec. Typical on time is 3µsec and typical on-off time is 50-60µsec.

Q. Can I parallel my outputs?

A. Any or all of the 8 module outputs can go to the same output device, as long as the output commons and Vcc are the same.

Q. Can I parallel my inputs?

A. You can parallel inputs if the device can supply enough current to drive multiple inputs.

Q. If I have different sources of power for my input devices, will I have input common problems?

A. You don't need to tie commons together. The isolation between channels is large enough to eliminate common mode voltage problems.

Q. If I set both the preset and reset bits to one counter in one BTW, what will happen?

A. The preset has priority, so only the preset will occur. The outputs will follow the preset.

Q. If I change the BTW configuration data, how long will it take for the module to process the changes and execute them?

A. It depends on the length of the BTW. The module spends about 80µsec decoding each word of new data in binary. It takes twice as long to decode BCD. A worst case example of 64 words will take about 5.5msec in binary, and 11msec in BCD. These times start after the module receives the BTW. Don't forget that it may take additional time based on changes in rate measurement sample periods. If you changed the sample period to 2 seconds, it will take an additional 2 seconds to receive a new frequency value.

Q. In frequency mode, how are my samples taken?

A. In rate measurement, you select a time period in BTW words 21-24. The module will count pulses on channel A for this time period, and then convert the number to frequency. It will begin its next time period in about 10msec, and then begin counting pulses again.

In period/rate or continuous/rate modes, the pulses coming in on the gate/reset will gate the internal 4MHz clock using the hardware scaler selected in words 21-24. If a scaler of 1 is selected, you are measuring the number of 4MHz pulses that occurred while the gate/reset was active, and the frequency returned will only be accurate if the incoming pulses occur with a 50% duty cycle. With all other scaler values, you are measuring the number of 4MHz pulses that occur in the scaler during a number of gate/reset periods that equal the the scalar value. For example, with a scaler value of 8, the 4MHz clock will be measured for four periods. The frequency value, 4MHz count ND bit and outputs will then be updated and remain constant as the counter is idle for the next four periods. Then the 4MHz clock will be measured for the next four periods and then be idle for four periods. Thus, the frequency is updated every eight periods. For more information, refer to appendix E.

Q. How often is the BTR data updated at the module?

A. The data available to be read by the processor is updated every 1.5–2.9msec binary and every 3.0–5.8msec BCD. Note that based on module configuration, some values may not be updated at that rate. For example, a frequency value in rate measurement mode will be updated at the time base selected in the scaler word. The module can always be read by the processor, but if read at a faster rate than determined by the time base, you will read old data.

Q. How often can I do a BTW?

A. This varies with the length sent and whether or not any data has changed. The worst case would be a 64 word BTW that changes the module configuration. This would take about 5.5ms in binary (11.1ms in BCD) to process. You would not be able to do another BTW for that length of time. If the BTW data has not changed any module configuration on that particular scan, the rate at which you can do a BTW will vary (depending on module configuration) from about 1.5ms to 2.9ms. The best case configuration would be no channels in period/rate or continuous rate; worst case configuration would be all 4 channels in period/rate or continuous rate.

Q. How do my output on-off values work?

A. The first value is always the on value, and the second value is always the off value. For example, with a rollover value of 2000, if I specify an on value of 1999 and an off value of 0, the output will only be on when the count equals 1999. If I specify an on value of 0 and an off value of 1999, the output will only be off at a count of 1999.

Q. How do my outputs work if I tie them to an input used in frequency mode.

A. If an output is tied to an input used in period rate mode, the output will be triggered by the counts, not by the frequency. The module provides better resolution by tieing the output to the 4MHz clock count value instead of the frequency. For example, in period rate mode with a scaler value of 1, feeding the gate input a constant frequency of 285Hz will return a frequency of 284-285, but the counts returned will be 7017-7019. The output is tied to the count value of 7017-7019.

If an output is tied to an input used in rate measurement mode, the output is tied directly to the frequency. For example, with a time base of 500msec the count returned will be 142-143, and the frequency will be 284-286Hz. The output will be tied to the frequency 284-286Hz.

Q. If I change the on-off value of an output, how long before it takes effect?

A. If the output is tied to an input used in any of the count modes, the change will take effect at the end of the BTW processing time. The BTW processing time is based on the number of words sent (5.5msec binary and 11msec BCD for a 64 word transfer) after the BTW done bit is set.

If the output is tied to an input in either frequency mode, the output change will not take effect until the data is processed as above.

Q. What are the counts returned in rate measurement mode?

A. These counts are the number of counts received on channel A during the selected sample time period. The counts are divided by the specified time base and converted to frequency. For example, with a time base of 500msec and a fixed frequency of 285Hz on channel A, a count value of 142-143 will be returned, resulting in a frequency of 284-285.

Q. What are the counts returned in period rate mode?

A. These counts are the number of 4MHz internal clock pulses that occurred during the selected number of scaler gate pulses. Each pulse would be equal to the gate terminal being high for 0.25µsec.

Q. What happens if I change my BTW length after power up to save block transfer time?

A. As long as the length is valid, the module will retain the data previously sent to it as long as backplane power to the module is present. If you power up with a block transfer length of 64 words to configure the module, and later change to 2 words, the module will behave in the manner prescribed in the 64 word transfer. It will do this until you power down, and power back up. This configuration is not affected by switching your processor from RUN to PROG mode.

Q. How do I know what length to make my BTW file?

A. There are 3 approaches to consider: speed, functionality and occasional usage.

When considering speed, you would want to configure the module once, and then have access to certain BTW data only. You would power up with a configuration word length of 64 words for access to all data, and then change the length to just 2 words allowing you to access specific commands, such as preset or enable outputs. This would save BTW time by not sending data which is not changing.

In the second approach, functionality, you might not be using your outputs, so you would not need to have a 64 word BTW length. For example, if you just needed to preset counter 3, you would only need 20 words. You could then perform presets without sending unnecessary words.

Using the occasional usage approach, you could do BTWs only on occasion, such as when you needed to change output values. You could reanable the BTW long enough to send new data, and disable it thereafter.

Any or all of these approaches can be used to best suit your individual needs.

Period/Rate and Continuous/Rate Examples

General

The totalizer is always active in period/rate and continuous rate modes. To access the values, the BTR length must be changed to a value between 20 and 26 in multiples of 2. A length of 20 will return the total count for C0, a length of 22 will return the total count for C1 and C0, and so on. A BTR length of 0 will still return 18 words.

The reset bits will now reset the total count in words 19-26. The count will continue to accumulate until 999,999 and then rollover to zero. The presets and rollover in the BTW are inactive

When using the reset, you can always be off by (1–scaler). For example, with a scaler of 8 after issuing a reset, you may have only 1 pulse occur, but your count may immediately go to 8, making you off by 7 counts. Also, if you dynamically change the scaler, your count can be off by the larger of the new or old scaler, and changing the scaler will reset the count to 0.

The total count value will be updated every scaler number of pulses at the gate/reset pin.

The maximum allowable input frequency for the total count to be accurate varies with module configuration and the scaler by about 340–520Hz times the scaler.

For example, the best case is with only 1 channel operating in period/rate or continuous/rate modes.

scaler = 1	Frequency = 520Hz
scaler = 2	Frequency = 1040Hz
scaler = 4	Frequency = 2080Hz
scaler = 128	Frequency = 66.5KHz

For example, the worst case is with all 4 channels operating in period/rate or continuous/rate modes.

scaler = 1	Frequency = 340Hz
scaler = 2	Frequency = 630Hz
scaler = 4	Frequency = 1260Hz
scaler = 128	Frequency = 43.5KHz

The above is only true if you are not doing BTWs, the BTW length is less than 3, or the data in the BTW does not change for any counter.

When doing BTWs whose length is greater than 3 or if the BTW data changes, the potential to miss pulses is limited to (number of pulses in 6ms – scaler) every time there is a transition of BTW data if the number pulses that occur in 6ms is greater than scaler. If the number of pulses that occur in 6ms is less than the scaler, the count will remain accurate.

There is no minimum limit to the input pulse width as long as no more than the scaler number of pulses appear in (1/above allowable input frequency) seconds.

It is important to note that even if the above frequency is exceeded the 4MHz count and frequency will still be accurate. Only the total counts returned will be unreliable.

Changes made in Revision B

The following are changes made to the 1771-VHSC module in revision B.

Period/Rate mode mode has been modified such that if the pulses at the gate/reset stop, the frequency (BTR words 11–18) will go to zero and the 4MHz count (BTR words 3–10) will go to 999,999.

Continuous/rate mode has been added. This mode operates identical to period/rate mode with the exception of the outputs.

If the frequency is very near (scaler x 2Hz), the most significant digits of the 4MHz count can be greater than 999. This value will be accurate.

In period/rate and continuous/rate modes, the smallest frequency returned equals (2 x scaler)Hz. Frequencies less than this will return 0Hz.

The frequency will go to 0 and the 4MHz count will go to 999,999 250–260ms after the last pulse. The new data bit will also be set.

Words 19 through 26 have added to the BTW.

Operation of Outputs in Period/rate Mode (1771-VHSC Revision B Modules)

The following examples demonstrate the operation of the outputs in period/rate mode of operation for the 1771-VHSC revision B modules.

1. If scaler = 1

The 4MHz count, frequency, new data bit, totalized count and outputs will be updated on the trailing edge of every pulse at the gate/reset input.

2. If scaler ≠ 1 and (Number of pulses occurring in 250ms) < (1/2 scaler + 1)

The 4MHz count will remain at 999,999, the frequency will remain at 0. The outputs will be on if A (output on preset) > B (output off preset). The outputs will be off if A (output on preset) < B (output off preset).

3. If scaler ≠ 1 and (1/2 scaler + 1) ≤ (Number of pulses occurring in 250ms) < (1.5 scaler)

The outputs, 4MHz count, frequency, and new data bit will be updated on the leading (not inverted) edge of the scaler + 1 number pulse occurring in 250ms.

Note: Any previous pulses less than the scaler number that occurred at any time will effect the module update. For example, with a scaler of 4, and applying six pulses every 300ms at the gate/reset terminal, the module will do an update every other burst of six pulses because there are “left over” pulses from the previous burst.

4. If scaler ≠ 1 and (Number of pulses occurring in 250ms) ≥ 1.5 scaler

The outputs, 4MHz count, frequency and new data bit will be updated on the leading edge (not inverted) of the scaler + 1 number pulse.

In all cases, if the incoming pulses stop the 4MHz count will go to 999,999, the frequency will go to 0, the new data bit will be set, and the outputs will be updated accordingly 250–260ms after the last pulse.

If the pulses have stopped for more than 250ms the first time that the output should be updated, it will occur within 1.5ms (3ms in BCD) of the actual pulse.

The totalized count is updated every scaler number of pulses, but due to “left over” pulses may increment by more than the total number of pulses that occurred. For example, with a scaler of 2 and the gate/reset terminal receiving 3 pulses every 300ms, the total count will increment by 4 every fourth burst of pulses.

Note: “Left over” pulses are pulses that occur that are not divisible by the scaler. (i.e. With a scaler of 4, if 6 pulses occur there are 2 “left over” pulses.)

Operation of Outputs in Continuous/Rate Mode

The following example demonstrates the operation of the outputs in Continuous/Rate mode of operation. Note that Y = time between incoming pulses trailing edge to leading edge, A = output on value, and B = output off value.

The examples shown assume that, at the least, the number of pulses equal to the scalar value is occurring at the gate/reset pin.

1. A < 4MHz count and B <> 0 and A > B

Output on time = (4MHz count – A) 250ns + scaler (Y) + (B)(250ns)

2. A > 4MHz count and B <> 0 and B < 4MHz count and A > B

Output on time = scaler(Y) + B(250ns)

3. A > 4MHz count and B <> 0 and B > 4MHz count and A > B

Output = On

4. A > 4MHz count and B = 0

Output = Off

5. A < 4MHz count and B = 0

Output on time = (4MHz count – A)250ns

6. A < B < 4MHz count and A <> 0

Output on time = (B – A)250ns

7. A < 4MHz count < B and A <> 0

Output on time = (4MHz count – A)250ns

8. (4MHz count < A < B) or (A < B and 4MHz count > B) and A <> 0

Output = Off

9. (B > 4MHz count) or (B > 0 and 4MHz count = 999,999) and A = 0

Output = On

10. B < 4MHz count and A = 0

Output off time = (4MHz count – B)250ns

The 4MHz count, total count, frequency and new data bit reported to the programmable controller will be updated every scaler number of pulses. And 250–260ms after the last pulses stop, the 4MHz count will go to 999,999, the frequency will go to 0 and the new data bit will be set. The outputs are updated dynamically on the module as the 4MHz count increases.

If less than the scaler number of pulses occurs in 250ms, but at least 1/2(scaler) + 1 pulses occur in 250ms, the operation of 4MHz count and frequency will be accurate, but may appear intermittent due to "left over" pulses. The outputs will always update every scaler number of pulses regardless of the update of the 4MHz count.

Note: "Left over" pulses are pulses that occur that are not divisible by the scaler. (i.e. With a scaler of 4, if 6 pulses occur there are 2 "left over" pulses.)

Examples of Period/Rate and Continuous/Rate

The following waveforms illustrate the difference between period/rate and continuous/rate. All waveforms were initiated by applying a 50Hz signal at the gate/reset terminal of a counter configured for either period/rate or continuous/rate. The output configuration remained constant with an ON value of 20,000 counts and an OFF value of 80,000 counts. Only the scalar mode was varied to show the operation of the two modes.

Figure E.1
Operation of Outputs in Period/Rate and Continuous/Rate with Scaler = 1

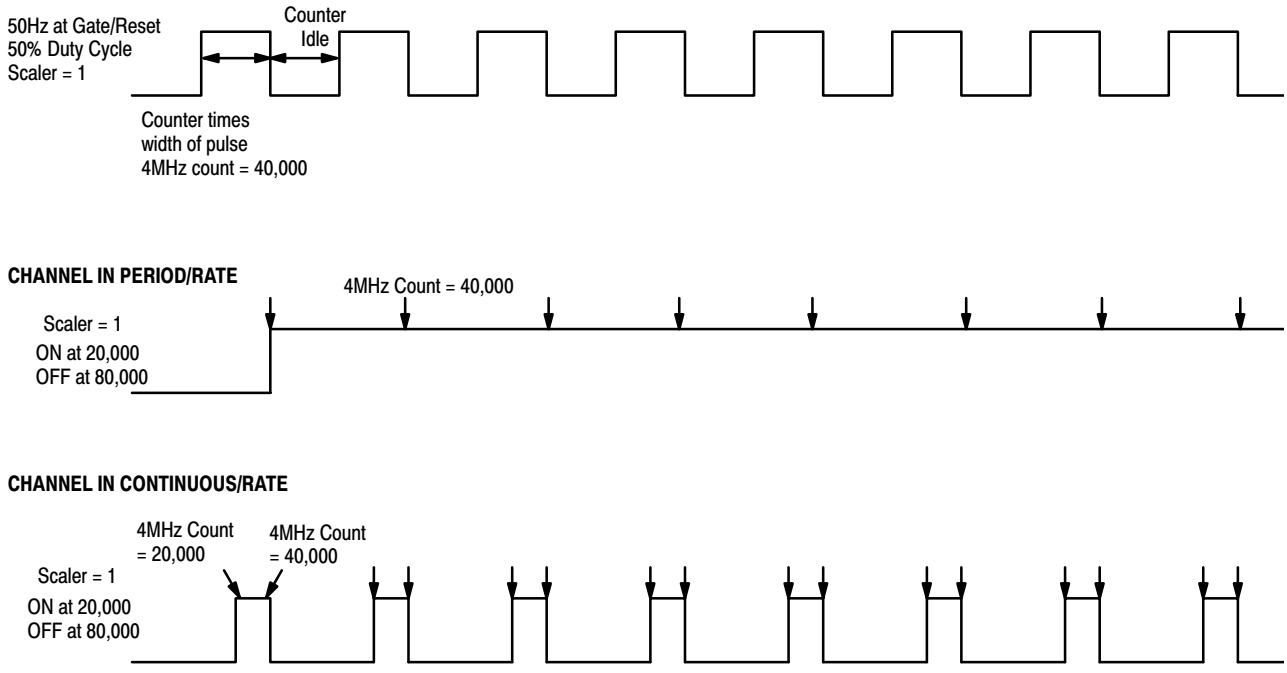


Figure E.2
Operation of Outputs in Period/Rate and Continuous/Rate with Scaler = 2

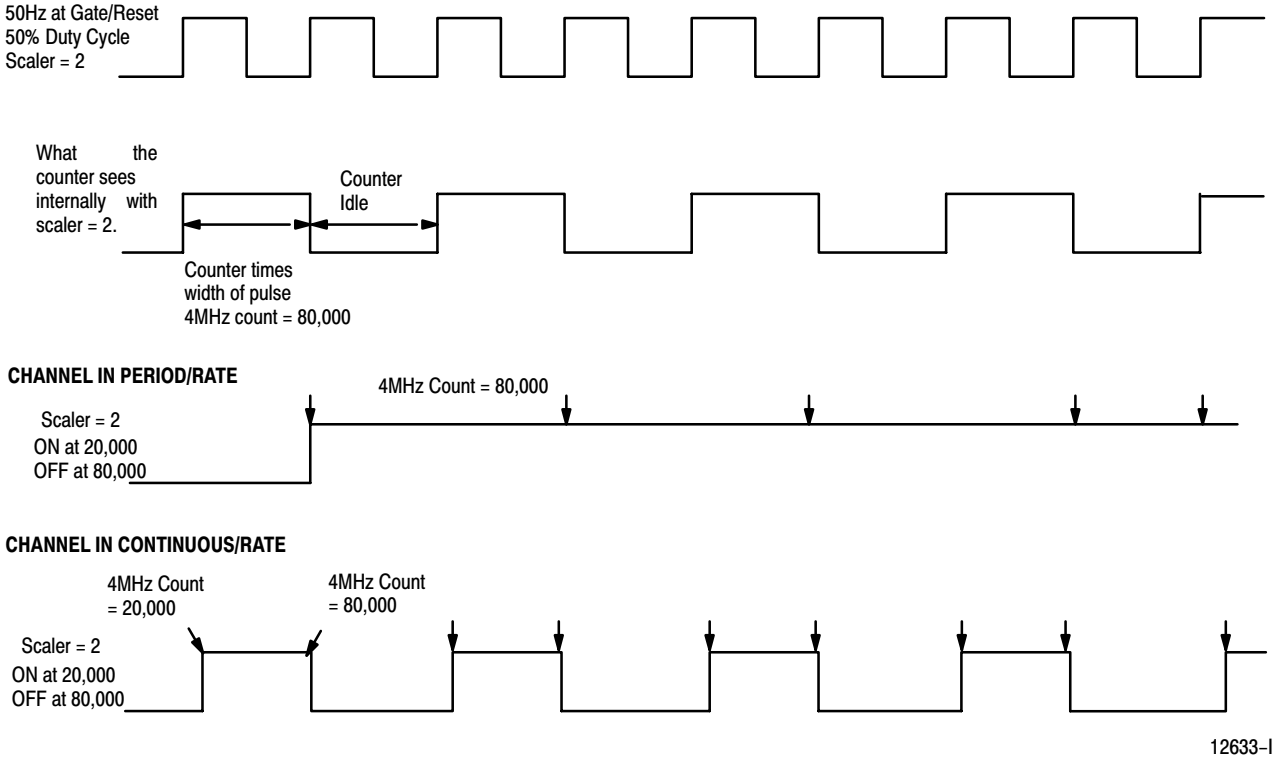


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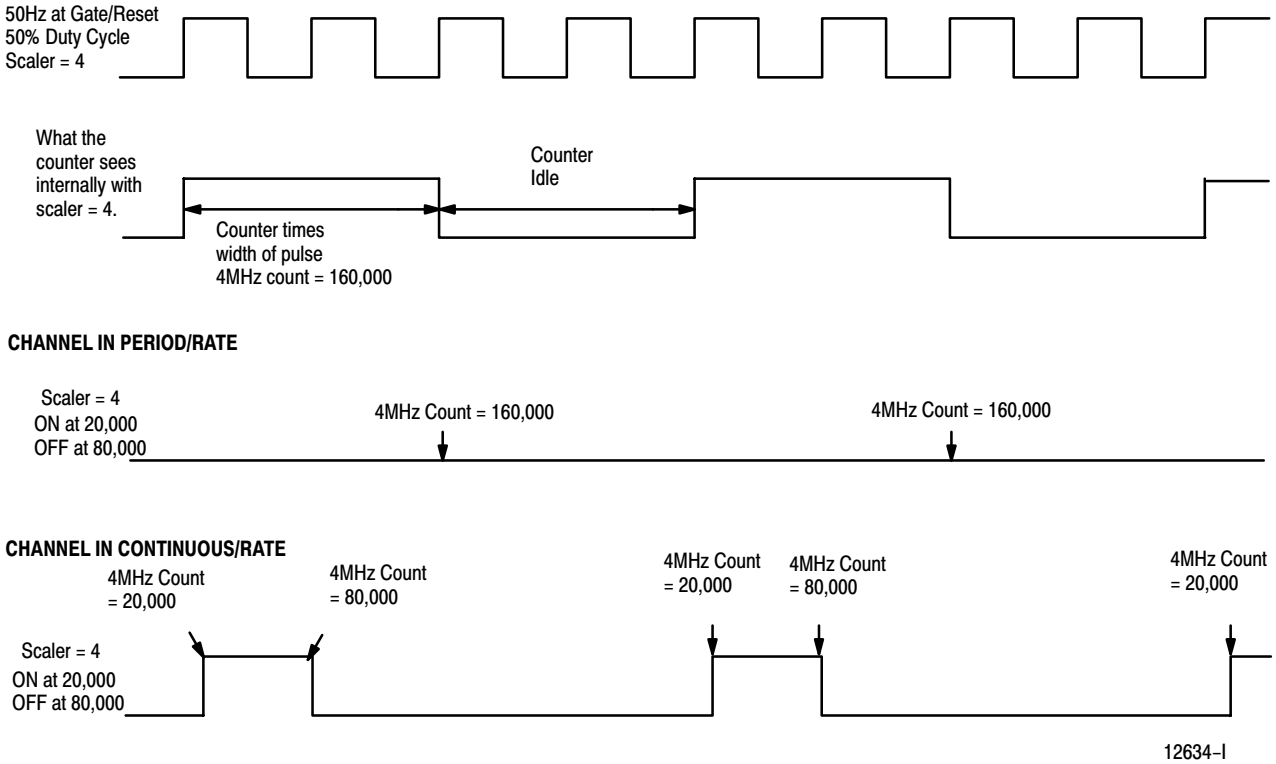
Figure E.3
Operation of Outputs in Period/Rate and Continuous/Rate with Scaler = 4



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